This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTIE.2021.3074864, IEEE Journal of Emerging and Selected Topics in Industrial Electronics

A New High Gain, High-Efficiency SEPIC-Based DC-DC Converter for Renewable Energy Applications

S. Hasanpour, M. Forouzesh, *Student Member, IEEE,* Y. P. Siwakoti, *Senior Member, IEEE,* F. Blaabjerg, *Fellow, IEEE*

Abstract—This paper proposes a new configuration of Quasi-Resonant High Gain, High-Efficiency Single Ended Primary Inductor Converter (QRHGHE-SEPIC)-based DC-DC converter with continuous input current. The presented single-switch topology uses a Coupled-Inductor (CI), a Voltage Multiplier (VM) integrated with a regenerative passive lossless clamp circuit to enhance the voltage conversion ratio. In the proposed converter, the main power switch turns on at Zero Current Switching (ZCS). Moreover, by adopting a Quasi-Resonance (QR) operation between the leakage inductor of the CI and the middle capacitors, the current value of the main switch at turn-off moment is alleviated. In addition, the leakage inductance slows down the turn-off slope of all diodes and hence there is no reverse recovery problem in the proposed converter. Due to soft-switching operation in all switching components, the power dissipations in the converter are significantly alleviated. Thus, the proposed QRHGHE-SEPIC can provide high voltage gain whilst achieving a high efficiency. Steady-state analysis, comprehensive comparisons with other related converters and design considerations are discussed in detail. Finally, to verify the validity of the theoretical analysis, a 160 W/ 200 V sample prototype is demonstrated at the switching frequency of 60 kHz and with voltage gain of 10.

I. INTRODUCTION

Various types of Renewable Energy Sources (RES), such as fuel cells (FCs), Photovoltaic (PV) panels, and wind turbine are increasingly developing and becoming prevalent in modern society. Nowadays, high voltage gain switched-mode DC-DC converters are imperative for interfacing the low voltage RES (typically <50 V) to reach an appropriate DC bus voltage. In this step-up converter application, current-fed topologies with low input current ripple are a more appropriate choice compared to the voltage-fed ones as they ease the maximum power extraction from the RES [1]. For low power applications and where electrical isolation is not mandatory for the power conversion stage, non-isolated step-up DC-DC converters with proper performance indicators including high voltage gain, low voltage stress, high efficiency, continuous input current, small volume, and low cost are more desirable than the isolated ones.

The conventional step-up DC-DC converters such as boost and SEPIC converters with a simple structure are theoretically able to provide a high voltage gain for the RES. However, in practice, high voltage stress across the main power switch and considerable reverse recovery loss limit the step-up ratio and converter efficiency significantly in such converters, especially in high voltage applications [2]. Due to these drawbacks, it is necessary to modify the configuration of step-up DC-DC converters to improve the performance indicators.

For this purpose, to increase the voltage gain ratio of the conventional DC-DC converters, some effective voltage boosting strategies such as Voltage Lift (VL), Voltage Multipliers (VM), Switched-Capacitors/Inductors (SC/SI), and also Cascading Techniques (CT) are applied in [2] and [3]. Although these modified converters can achieve a high voltage gain, using a large number of passive components and operating in hard-switching condition, which limits the efficiency severely [4].

In recent years, the most widely investigated field of step-up DC-DC converters with high voltage gain is related to the implementation of magnetic components. For this purpose, Coupled-Inductors (CIs) and/or transformers are broadly employed in different configurations to achieve a wide range of voltage gain by adjusting the winding turns ratio [2]. However, in many CI-based converters, the energy stored in the leakage inductor of the CI causes high voltage spikes across the switching components, which leads to reduced efficiency. To recover this energy from the leakage inductor, active or passive clamp networks can be used [5] and [6]. In higher voltage applications such as in motor drive, space/satellite, and UPS, other voltages boosting strategies (VL, VM, SC/SI, and CT) are also employed in CI-based DC-DC converters to further enhance the output voltage [3]. However, the use of CI at the input in series with DC voltage source creates a large current ripple [7]. It is noteworthy that many CI step-up DC-DC converters with a high voltage conversion ratio have been presented in scientific papers [2], [3]. However, many of these converters suffer from high voltage stress, high switching loss, and diode reverse recovery loss, which limit their practical implementation due to the compromised conversion efficiency. To overcome the mentioned drawback, soft-switching step-up converters are becoming more popular.

So far, many CI boost-based converters with high voltage gain have been presented in [2], [3], [5], and [8]. Nevertheless, to achieve the soft-switching conditions in these converters, it is often required to use an auxiliary circuit (an additional clamp or snubber), which often increases the design complexity, cost, and weight [9] and [10]. In addition, in some types of these soft-switching converters, the voltage gain is a function of several converter parameters such as duty cycle, phase shift, and frequency that complicates the design and control of the converter [11] and [12].

In addition to the conventional boost converter, the SEPIC converter can also be used to increase the voltage of the RES. One of SEPIC's unique features is the possibility to create a Quasi-Resonant (QR) operation through a resonant tank between the middle parameters (the balancing capacitor and the parallel inductor) during the turn-on mode of the switch. Therefore, the soft-switching performance can obtain for the power switch without adding auxiliary elements, which improves the efficiency of the converter in comparison to the boost-based converters.

Recently, various modified DC-DC structures of SEPIC converter using CI and other voltage boosting techniques have

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTIE.2021.3074864, IEEE Journal of Emerging and Selected Topics in Industrial Electronics

been presented. In [5], by replacing a CI with the middle inductor of the SEPIC, the voltage gain is slightly enhanced. In this converter, a simple passive clamp circuit (diode and capacitor) is used to recycle the leakage energy of the CI. Another SEPIC-based step-up converter utilizing two pairs of CI is suggested in [13]. Even though an ultra-high voltage gain is obtained, this converter suffers from high input current ripple, voltage stress, and high value of the switching and reverse recovery power dissipations. In the SEPIC converters proposed in [14] and [15], by using VMs in the form of a voltage rectifier on the secondary side of the CI, the voltage gain is increased significantly. Nevertheless, the use of many components is the main drawback of these converters. Two new types of single-switch SEPIC-based converters using CI, VM, and clamp circuits with high voltage gain and low reverse recovery loss are presented in [16] and [17]. However, the major demerit of these converters is the high input current ripple. In [7] and [18], new types of CI SEPIC-based converter using clamp capacitor with low switching power losses are presented. Despite achieving a high voltage gain, high input current ripple is a great disadvantage of these converters, which limits their application for the RESs. Moreover, new double switch step–up SEPIC converters with low voltage stress are suggested in [19] and [20]. In these converters, using an active clamp capacitor, zero voltage switching (ZVS) condition is provided for the main power switch. Moreover, in [21]-[23] new types of CI SEPIC converter with regenerative passive clamp circuits are presented. In these converters, switching components are derived under low voltage stress. In addition, the leakage inductor of the CI helps to decrease the reverse recovery loss of the diodes. However, these converters cannot provide a wide range of output voltage. Moreover, in [24]-[27] several types of single-switch SEPIC based converters with continuous input current and high efficiency are proposed. In these converters, inherent property of the SEPIC is used to create a QR performance without any additional auxiliary components, and hence the switching and diode reverse recovery losses are alleviated significantly. Nevertheless, the voltage gain ratio is not sufficiently enhanced. Furthermore, a high voltage gain SEPIC-based DC-DC converter with continuous input current is suggested in [28]. In this converter an active auxiliary switch helps to achieve ZVS for main power switch. In addition, in [29], a new high voltage gain topology with high input current ripple using only six components is presented. Because of the voltage gain ratio in this converter is positive in the limited range of $0<D<0.25$ with a very sharp slope, Which leads to more complex control.

Regarding the aforementioned aspects in the development of high step-up DC-DC converters, the objective of this paper is to propose a new QR High-Gain, High-Efficiency SEPIC (QRHGHE-SEPIC)-based DC-DC converter. The outstanding features of the proposed QRHGHE-SEPIC are high voltage gain, continuous input current with low ripple, low voltage stress on semiconductor components and soft-switching performance (in the form of ZCS) for single power switch and all diodes of the converter. Employing a VM and a CI in the middle stage of the circuit allows to achieve high voltage gain ratio without using large duty cycles. In the proposed converter, the single power switch turns on under ZCS condition. Also, the QR performance leads to a decrease in the switch current value at the turn-off instant, thereby leads to diminishing the turn-off power loss. Moreover, the leakage inductor causes the ZCS condition at the turn-off time for all diodes that leads to eliminating the reverse recovery power losses from diodes.

This paper is organized as follows. The proposed QRHGHE-SEPIC is introduced in Sections *II* and *III* with a comprehensive operational analysis. Performance assessment of the proposed topology is presented in Section *IV*. Section *V* explains the design procedure of the elements. Finally, experimental results from the laboratory prototype validate the performance and mathematical derivations of the presented converter in section *VI*.

II. Circuit Description of the QRHGHE-SEPIC

The equivalent circuit of the proposed QRHGHE-SEPIC is shown in Fig. 1. The converter is composed of a CI with turns ratios of n, a single power switch (S), an input inductor (L_{in}), four diodes (D_1-D_3 and D_o), and five capacitors (C_1-C_4 and C_o). Series interconnection between the input inductor and input DC voltage source leads to low input current ripple, which improves the RESs performance. Moreover, the maximum voltage rate across the single switch is restrained by a regenerative passive lossless clamp circuit including C_2, C_3, and D_2 as seen in Fig. 1. Therefore, a switch with low static drain-to-source ON-resistance ($R_{DS(on)}$) can be used, which reduces the conduction power losses. The combination of the secondary side of the CL along with capacitors C_2 and C_4, and diodes D_1, D_2, and D_3 form a VM to increase the voltage gain in the low turns ratio of the CI. Moreover, the current waveform of the switch and the diode D_3 change in sinusoidal form because of a QR operation among the leakage inductance of the *CI*, C_1, C_3, and C_4. This also helps to reduce the switch turn-off and the reverse recovery losses. To simplify the converter analysis in Continues Conduction Mode (CCM) condition, the following assumptions are considered:

1) All switching components of the converter are ideal without parasitic components.
2) All capacitors are large enough so that their voltages are constant.
3) The CI is modeled by a parallel magnetizing inductor (L_M) and a series leakage inductor (L_k) seen from the primary side with a turns ratio of $n=n_2/n_1$.
4) The input and magnetizing inductors are considered to be large enough so their current ripple is negligible.

Fig. 2 depicts the main theoretical waveforms of the proposed QRHGHE-SEPIC for a switching period. These key

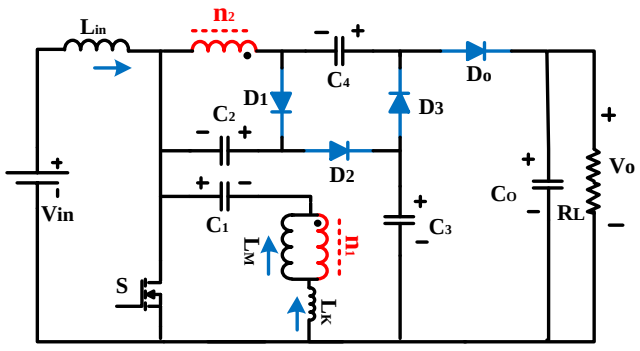


Fig. 1. The proposed QRHGHE-SEPIC -based DC-DC converter.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTIE.2021.3074864, IEEE Journal of Emerging and Selected Topics in Industrial Electronics

waveforms are broken down into six operating intervals at time duration ranges from t_0-t_6. The equivalent circuit for each operating mode is shown in Fig. 3.

Mode I [t_0-t_1]: At the beginning of this transient mode, at $t=t_0$, the power switch S turns on at ZCS condition. In this mode, the input inductor and the magnetizing inductor start charging from the input DC source and the capacitor C_1, respectively. Then, their current increases linearly in this mode. Diodes D_o and D_1 are conducting in this time duration. Since the leakage inductor current in the secondary side of the CI is decreasing, the current through D_o and D_1 starts to decrease linearly. At the end of this mode, the current of the output diode D_o reaches zero with a low reverse recovery (LRR) problem. The following equations can be expressed in this time interval:

$$v_{LM} = v_{c1} \quad (1)$$
$$v_{Lin} = V_{in} \quad (2)$$
$$V_{out} = v_{C2} + v_{C4} \quad (3)$$
$$i_S = i_{in} + i_{LK}\text{-}i_{n2} \quad (4)$$

Mode II [t_1-t_2]: In this time interval, the power switch S along with the diode D_1 remain on. The current of the input and magnetizing inductors increase linearly like in Mode *I*. The capacitor C_2 receives energy from the magnetizing inductor. This stage ends when the current of the diode D_1 reaches zero at LRR condition. Moreover, at the end of this mode, the energy of the output capacitor C_o starts transferring to the output load.

Mode III [t_2-t_3]: At time t_2, the diode D_3 starts conducting at ZVS condition. Thus, a resonance between the leakage inductor L_k and the capacitors C_1, C_3, and C_4 occurs in the form of QR, which discharges the energy of the capacitor C_3 into the balancing capacitor C_4. With the help of this resonant tank, the current in the switch S, the diode D_3 as well as the leakage inductance has a sinusoidal shape. This leads to a decrease in the current value of the power switch at the end of this time interval, which reduces its turn-off loss. The resonant frequency (f_R) is obtained as follows:

$$f_R = \frac{1}{T_R} = \frac{1}{2\pi\sqrt{L_k[C_1 \| (n^2(C_3 \| C_4))]}} \quad (5)$$

In this time interval, the following equations can be written:

$$v_{LM} = v_{c1} \quad (6)$$
$$v_{L1} = V_{in} \quad (7)$$
$$v_{C4} = v_{C3} - nv_{LM} \quad (8)$$
$$i_S = i_{in} + i_{LK} + i_{D3} \quad (9)$$

It is noteworthy that, to eliminate the reverse recovery loss of the diode D_3 and decrease the switch turn-off loss, it is necessary that the resonant time (T_R) is less than the pulse width of the switch ($T_R/2 \leq D \times T_s$) as seen in Fig. 2. Same as the previous modes, the input and the magnetizing inductors receive energy from the input source and capacitor C_1, respectively.

Mode IV [t_3-t_4]: This mode starts when the resonance between the leakage inductance L_k and the capacitors C_1, C_3, and C_4 is finished and the current of the diode D_3 reaches zero under ZCS condition without a reverse recovery problem. In this mode, all diodes are in reversed bias. Referring to Fig. 3 (d), the leakage and the magnetizing inductors have identical current. The current of the power switch is expressed as follows:

$$i_S = i_{in} + i_{LM} \quad (10)$$

Mode V [t_4-t_5]: At time $t=t_4$, single power switch S is turned off and the clamp diode D_2 is forward biased as shown in Fig. 3 (e). Therefore, the voltage rate across the single power switch is restricted by capacitors C_2 and C_3. Moreover, in this stage, the output diode D_o along with diode D_1 start to conduct. Owing to the existence of the leakage inductor, the current of the diodes D_o and D_1 increase slowly under ZCS condition. Moreover, the capacitor C_2 receives energy from the magnetizing inductor. Furthermore, the clamp capacitor C_3 begins to charge from the input inductor current until the current of the D_2 reaches zero. Also, the capacitor C_4, the magnetizing inductor of CL, and the input inductor transfer their energy to the output capacitor. The following equations can be expressed in this mode:

$$v_{L1} = v_{in} + v_{C2} - v_{C3} \quad (11)$$
$$v_{LM} = v_{C3} - v_{C1} - v_{C2} \quad (12)$$
$$v_{out} = v_{C3} + v_{C4} \quad (13)$$

Mode VI [t_5-t_6]: At the beginning of this time interval, the current of the clamp diode D_2 reaches zero naturally, with a low reverse recovery loss. Same as Mode *V*, the energy stored in the input and magnetizing inductors along with balancing capacitor C_4 are transferred to the output. Thus, the current of the input and magnetizing inductor decreases linearly. The reflective load current on the primary side of the CI (i_{n1}) leads to a negative leakage inductor current. This provides ZCS conditions for the power switch in Mode I.

III. DESIGN EQUATIONS

A. Voltage Gain

To simplify the steady-state analysis of the presented circuit, short transitions that happen during switching can be ignored. Moreover, the voltages across all the capacitors are considered

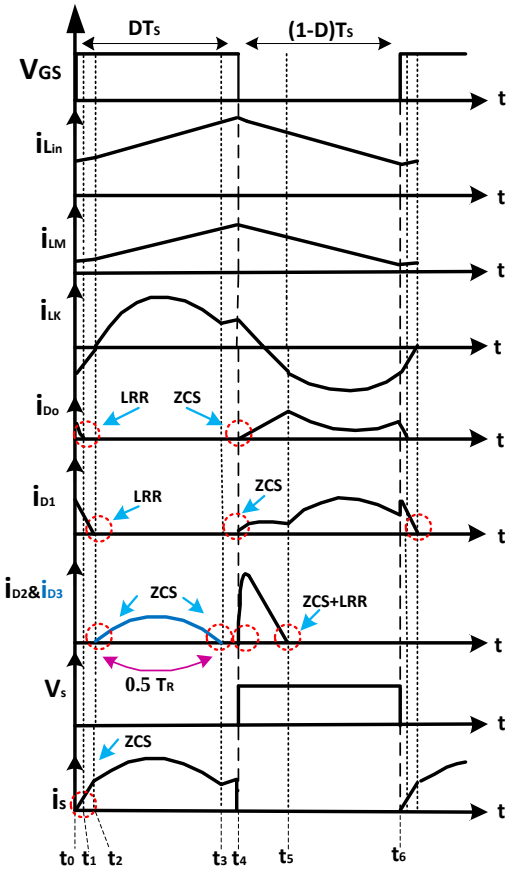


Fig. 2. The typical waveforms of the proposed QRHGHE-SEPIC. (**ZCS** = Zero Current Switching, **LRR**= Low Reverse Recovery.)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTIE.2021.3074864, IEEE Journal of Emerging and Selected Topics in Industrial Electronics

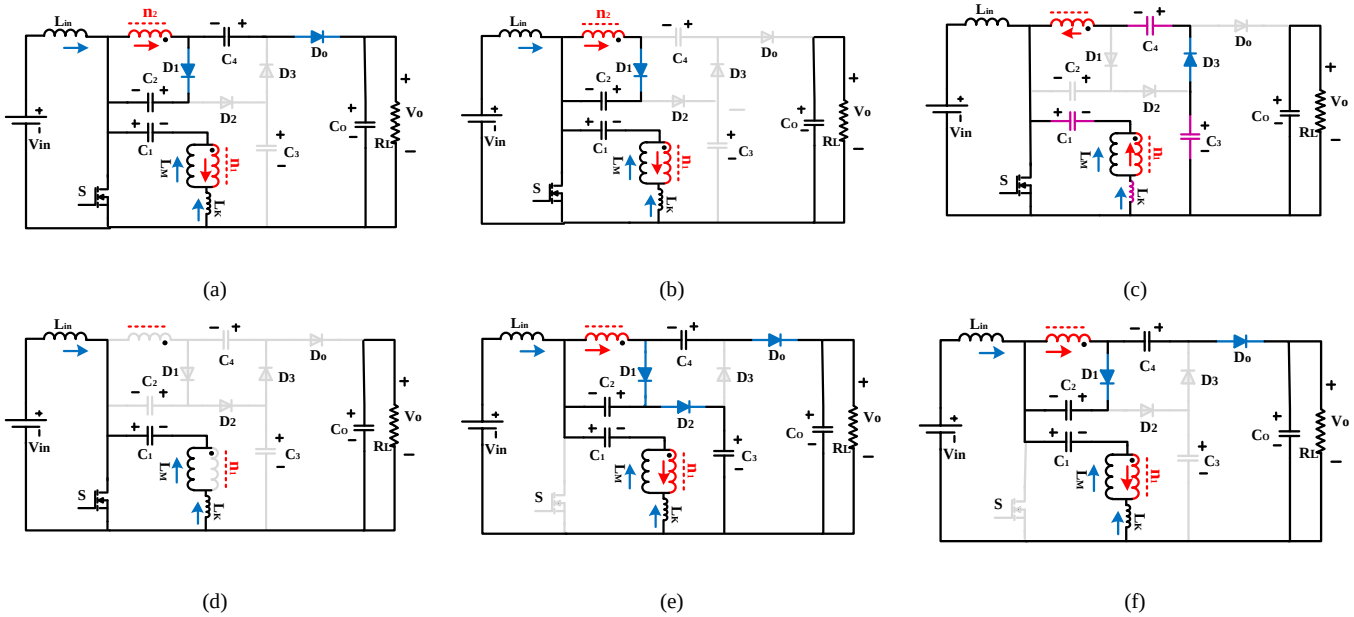


Fig. 3. The operation modes of the proposed converter, (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V, and (f) Mode VI.

to be constant. To calculate the voltage of the capacitors C_1 and C_2, the volt-second balance law are applied on the input and magnetizing inductors. Thus, the average value of capacitor voltages can be found as follows:

$$V_{C1} = V_{in} \tag{14}$$

$$V_{C2} = \frac{nD}{1-D} V_{in} \tag{15}$$

where D is the duty cycle of the main power switch and n is the CI turns ratio. In respect to operating Modes *III* and *V* and using (14) and (15), the voltage of the capacitors C_3 and C_4 are derived as:

$$V_{C3} = \frac{1+nD}{1-D} V_{in} \tag{16}$$

$$V_{C4} = \frac{1+n}{1-D} V_{in} \tag{17}$$

By substituting (16) and (17) into (13), the ideal voltage conversion ratio of the QRHGHE-SEPIC in CCM condition is obtained as:

$$M_{CCM(ideal)} = \frac{2+n(1+D)}{1-D} \tag{18}$$

Fig. 4 depicts the voltage gain ratio of the proposed converter as a function of the duty cycle and the different turns ratio of the CL. It can be seen that the voltage gain is directly increased proportionally and exponentially versus n and D, respectively.

B. *Voltage and Current Stresses*

The maximum voltage and current rate across the switching components strongly affect the possible choices for converter devices with minimum parasitic components. Drain-Source voltage stress (V_{DS}) across the main power switch (S) as a function of the output voltage and turns ratio of the CI can be given using the volt-second balance on the input inductor as follows:

$$V_{DS} = \frac{V_o}{2+n+nD} \tag{19}$$

In addition, the maximum repetitive peak reverse voltage across the converter diodes at their off-state are calculated as:

$$V_{D1} = \frac{nV_o}{2+n+nD} \tag{20}$$

$$V_{D2} = \frac{V_o}{2+n+nD} \tag{21}$$

$$V_{D3} = V_{Do} = \frac{1+n}{2+n+nD} V_o \tag{22}$$

According to equations (19)-(22), the voltage stress across the semiconductor devices can be reduced by a suitable selection of the CI turns ratio. Fig. 5 depicted the normalized voltage stress across the single power switch of the proposed converter as a function of the duty cycle for different turns ratios n of the CI. Regarding this figure, the voltage stress on the power switch is reduced by increasing the duty cycles and the turn ratios of the CI.

Using (18), the average value of the input inductor current is given as:

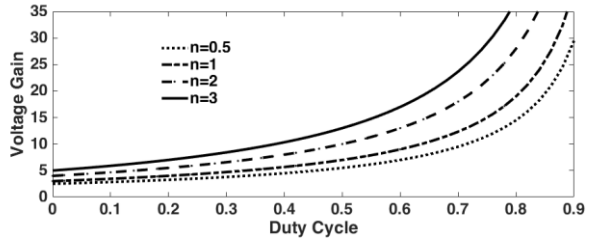


Fig. 4. Voltage gain as a function of duty cycle and turns ratio n.

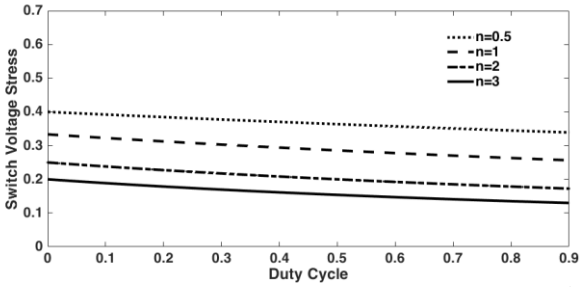


Fig. 5. The normalized voltage stress across the main power switch of the proposed converter as a function of the duty cycle for different turns ratios n of the CI.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTIE.2021.3074864, IEEE Journal of Emerging and Selected Topics in Industrial Electronics

$$< i_{in} >= MI_o \quad (23)$$

where I_o is the output load current. In addition, by applying the ampere-second balance principle for converter capacitors, the average current values of the diodes D_0, D_1, D_2, D_3, and the leakage inductance (L_k) can be obtained as follows:

$$< i_{D1} >=< i_{D2} \geq =< i_{D3} >=< i_{DO} >=< i_{LK} >= I_o \quad (24)$$

Considering the critical mode operation in QR operation which is taking place in Mode *III* ($T_R/2=D.T_S$), the averaged current passing through the magnetizing inductor (L_M) is calculated as follows:

$$< i_{LM} >= nI_o \quad (25)$$

The maximum current value passing through the clamping diode D_2 at the beginning of Mode *IV* is given as:

$$i_{D2(peak)} \approx (M+n)I_o = \frac{2+2n}{1-D} I_o \quad (26)$$

Regarding the sinusoidal form of the current shape of the diode D_3, and considering (24), the peak current of this diode is given as:

$$i_{D3\_peak} \approx \frac{\pi}{2D} I_o \quad (27)$$

Also, the peak current of D_1 and D_o can be estimated as:

$$i_{D1\_peak} \approx i_{Do\_peak} \approx \frac{I_o}{1-D} \quad (28)$$

Using (9), (18), and (27), the peak current and the Root Mean Square (RMS) value of the main power switch current are calculated as follows:

$$i_S(\mathrm{t}) = (\mathrm{M}+n)I_o + \frac{(1+n)\pi}{2D} I_o \sin(w_r t) \quad (29)$$

$$I_{S\_peak} \approx (\frac{2+2n}{1-D} + \frac{(1+n)\pi}{2D}) I_o \quad (30)$$

$$I_{S(RMS)} \approx I_o \sqrt{\frac{((1+n)\pi)^2}{8D} + D\left(\frac{2+2n}{1-D}\right)^2 + (1+n)(\frac{2+2n}{1-D})} \quad (31)$$

Fig. 6 shows a comparison between the current stresses of the single switch of the proposed converter against the diodes. Moreover, Fig. 7 illustrates the peak current and the RMS values of the main power switch as a function of duty cycle and different values of the CI turn ratio for the proposed QRHGHE-SEPIC converter. As it can be observed, the minimum value of switch current stress is obtained in the duty cycle range $0.4<D<0.65$. Moreover, increasing the CL turns ratio, leads to a proportional increase in the current stress.

Moreover, Fig. 8 illustrates the current waveforms of the power switch and the diode D_3 during three possible modes of QR operation including below resonance area ($T_R/2<DT_S$), critical resonance area ($T_R/2 = DT_S$), and above resonance area ($T_R/2 > DT_S$). According to this figure, only below and critical resonance areas, the switch turn off loss is alleviated. In addition, because of slow *di/dt, the* diode D_3 turns-off without reverse recovery loss, which improves the converter efficiency further. It is worth to note that reducing the resonance cycle (T_R) increases the peak currents of the switch and the diode D_3. Consequently, operating around the critical resonance area has the best overall performance.

C. Efficiency Analysis

The power losses calculation occurring in different components of the proposed QRHGHE-SEPIC are discussed in this section. In the proposed converter, due to the soft-switching performance for main power switch and all diodes, the switch turn-on and diodes reverse recovery losses can be neglected.

Switch losses: The switch power losses of the proposed converter including turn-off and conduction losses are obtained as follows:

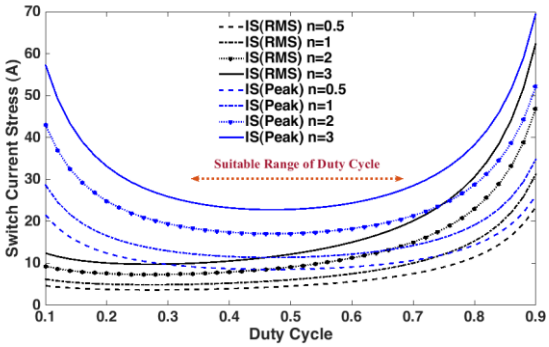


Fig. 6. Current stress of the power switch as a function of duty cycle and different turns ratio for Vo = 200 V and R_L=250 Ω.

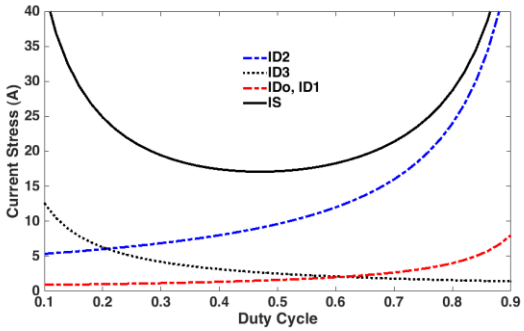


Fig. 7. Current stress of the switching components as a function of duty cycle under Vo = 200 V and R_L=250 Ω.

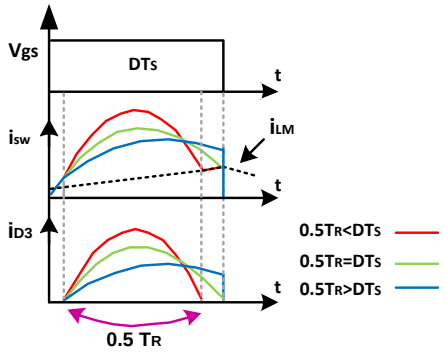


Fig. 8. Current shapes of the switch S and the diode D_3 under QR modes

$$P_{SW}^{loss} = \frac{1}{2T_s} . V_{DS}\left(i_{SW}^{\mathrm{t=off}} . t_{off}\right) + I_{S(RMS)}^2 . R_{DS(on)} \quad (32)$$

where t_{off} represents the turn-off transition time of the switch and I_{RMS} is the RMS value of the switch current. As mentioned before due to the below resonance operation the switch turn-off loss is alleviated in the proposed circuit.

Diode losses: The diodes power losses are related to the average current, forward voltage drop (V_F) and the conduction resistance (r_D), are given as:

$$P_{D_{1,2,3,o}}^{loss} = V_F . I_{D(AVG)} + I_{D(RMS)}^2 . r_D \quad (33)$$

Capacitor losses: The power losses of the capacitors that are caused by the equivalent series resistance (ESR) are estimated as:

$$P_{Capacitor}^{loss} = I_{C(rms)}^2 . ESR \quad (34)$$

Magnetic component Losses: The copper losses of magnetic devices (including L_{in} and L_m) can be expressed as:

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTIE.2021.3074864, IEEE Journal of Emerging and Selected Topics in Industrial Electronics

$$P_{magnetics}^{loss} = I_{L_{in}(RMS)}^2 \cdot r_{L_{in}} + I_{n1(RMS)}^2 \cdot r_1 + I_{n2(RMS)}^2 \cdot r_2 \quad (35)$$

where, r_1 and r_2 are the DC resistances of the primary and secondary sides of the CI, respectively.

Fig. 9 demonstrates the theoretical efficiency of the presented topology as a function of the duty cycle under several turn ratios of the CI ($n = 1, 2,$ and 3). The converter parameters are considered as follows:

$V_{in} = 20$ V, $R_L = 250\ \Omega$, $r_{Lin} = 40\ m\Omega$, $r_{LM\text{-}(n=1)} = 50\ m\Omega$, $r_{LM\text{-}(n=2)} = 70\ m\Omega$, $r_{LM\text{-}(n=3)} = 100\ m\Omega$, $f_s = 60$ kHz, $t_{d(off)} = 50$ ns, $t_{d(on)} = 26$ ns, $r_{ds(ON)} = 5.6\ m\Omega$, $r_{D1} = r_{D2} = r_{D3} = r_{Do} = 7\ m\Omega$, $r_{esrC1} = 25\ m\Omega$, $r_{esrC2} = 70m\Omega$, $r_{esrC3} = r_{esrC4} = 50\ m\Omega$, r_{esrCo}, $V_{FD1} = V_{FD2} = 0.47$, $V_{FD3} = V_{FDo} = 0.52$.

From this figure, Because of the high voltage and current rates in higher duty cycles, the efficiency is reduced. This sudden drop in the efficiency curve also happens in other high voltage gain topologies. However, the full soft-switching performance, which reduced the power dissipation, led to high power-handling capacity.

IV. PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER WITH OTHER SIMILAR TOPOLOGIES

In this section, a comparative analysis is done between the proposed QRHGHE-SEPIC and its counterparts that have been recently published. For this purpose, typical performance indicators of step-up DC-DC converters including the static voltage gain, components count, input current ripple, voltage stress, soft switching condition, and efficiency are evaluated in Table *I*.

Fig. 10 shows a line chart of the voltage gain comparison of the converters referenced in Table I under a specified turns ratio $n = 2.5$ for duty range $0<D<1$. As it can be seen, only converters [7], [8], [14], and [17] have higher voltage gain than the proposed converter. However, the use of larger number of components (in [14] and [17]), high input current ripple (in [7], [8] and [17]) are the main disadvantages of these converters, which limits their applications for the RESs. Also, the converter in [18], which has identical voltage gain with the proposed converter, suffers from a high input current. In the other cases, just the presented QRHGHE-SEPIC can provide a higher voltage gain compared to the other converters while maintaining low current ripple, low components count and soft-switching performance for power switch as well as very low reverse recovery loss.

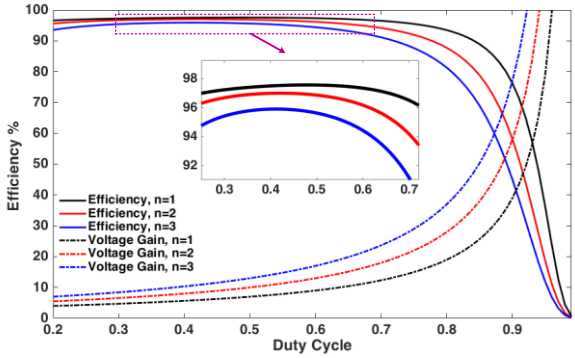


Fig. 9. The estimated efficiencies and voltage gains versus the duty cycle for different values of the turns ratios of the CI.

Furthermore, the normalized voltage stress rate across the power switch and the output diode of the converters that are given in Table *I* are compared under a specified condition ($n = 2.5$) and illustrated in Fig. 11 and Fig. 12. As it can be observed, the proposed QRHGHE-SEPIC has the lowest level of voltage stress compared to the converters with continuous input current and soft-switching performance. This makes it possible for the designer to use switching components with lower parasitic components (i.e. MOSFETs with lower $R_{DS(on)}$ and diodes with lower forward drop voltage V_F), which alleviates the power losses.

Moreover, due to the soft-switching performance in the proposed converter, the switching loss is negligible. Hence, it is expected the proposed converter can provide an ultra-high voltage gain under high efficiency. For this purpose, a comparison of the theoretical efficiency in the same conditions of the switching frequency, input and output voltages, and output load (20 V to 200 V/100 W/ 60 kHz and $n=2$) are carried out and shown in Table I. The Parasitic components (resistors and forward drop voltage) are selected identical in different converters based on related datasheets. Regarding this table, the proposed circuit demonstrates the highest efficiency against the converters that have a good performance for the RES.

Finally, based on the aforementioned discussions, the suggested QRHGHE-SEPIC with high voltage gain at high efficiency can offer relatively better performance for the RES applications than other topologies shown in Table I.

V. DESIGN PROCEDURE OF THE ELEMENTS

A. Turn Ratio of the CI and Duty Cycle

As mentioned in section *III*, proper selection of the turns ratio and duty cycle are very important to reduce the power losses that occur in the components. Regarding Fig. 5, the minimum values of the switch current stress occur in the duty cycle range $0.4 <D< 0.7$. After selecting the appropriate duty cycle range, using (18), the turns ratio of the CL (n) can be obtained as:

$$n = \frac{M(1-D)-2}{(1+D)} \quad (36)$$

B. Input (L_{in}) and Magnetizing (L_M) Inductances

To guarantee the best performance in RESs, it is necessary to draw continuous current with low ripple (CCM condition) from these sources. For this purpose, the input inductor L_{in} is designed as follows:

$$L_{in} = \frac{V_{in} \cdot D}{\Delta I_{in} \cdot f_s} \quad (37)$$

where ΔI_{in} is the permitted current ripple in the input inductor.

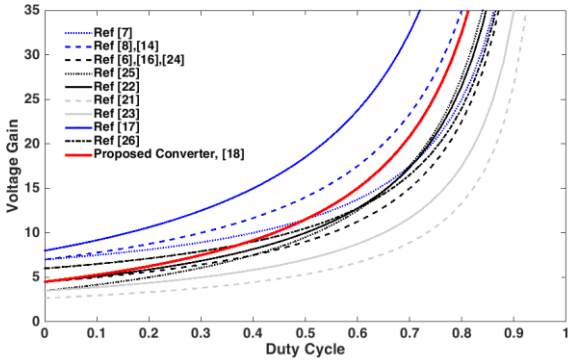


Fig. 10. Comparison of the voltage gain of converters mentioned in Table *I*.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTIE.2021.3074864, IEEE Journal of Emerging and Selected Topics in Industrial Electronics

TABLE I. PERFORMANCE COMPARISON OF DIFFERENT RELEVANT STEP-UP DC-DC CONVERTERS

Converter Topology	No. of Components S/D/C/CI+L/T	Voltage Gain	Input Current Ripple	Voltage Stress on Main Power Switch	Voltage Stress on Output Diodes	Soft-Switching (Switch)	Reverse Recovery Loss	Eff. 100Watt (60 kHz)
[6]	1/3/4/1+1/10	$\frac{n+2}{(1-D)}$	Low	$\frac{V_o}{n+2}$	$\frac{(1+n)V_o}{n+2}$	Yes	Medium	96.9%
[7]	2/3/4/1+0/10	$\frac{2+n(2-D)}{(1-D)}$	High	$\frac{V_o}{2+n(2-D)}$	$\frac{(1+n)V_o}{2+n(2-D)}$	Yes	Low	97.5%
[8]	2/4/5/1+0/12	$\frac{2(1+n)}{(1-D)}$	High	$\frac{V_o}{2(1+n)}$	$2\times\frac{V_o}{2}$	Yes	Very Low	97.5%
[14]	1/5/6/1+1/14	$\frac{2(1+n)}{(1-D)}$	Low	$\frac{V_o}{2(1+n)}$	$3\times\frac{1+2n(1-D)V_o}{2(1+n)}$	Yes	Low	94%
[16]	1/4/4/1+0/10	$\frac{n+2}{(1-D)}$	High	$\frac{V_o}{n+2}$	$\frac{(1+n)V_o}{n+2}$	No	High	95.3%
[17]	1/6/6/1+0/14	$\frac{3+2n+nD}{(1-D)}$	High	$\frac{V_o}{3+2n+nD}$	$\frac{(1+n)V_o}{3+2n+nD}$	Yes	Low	92%
[18]	1/4/4/1+0/10	$\frac{2+n+nD}{(1-D)}$	High	$\frac{V_o}{2+n+nD}$	$\frac{(1+n)V_o}{2+n+nD}$	Yes	Low	95.8%
[21]	1/3/4/1+1/10	$\frac{(2n-1)}{(n-1)(1-D)}$	Low	$\frac{(n-1)V_o}{(2n-1)}$	$\frac{nV_o}{(2n-1)}$	Yes	Low	94.8%
[22]	1/4/5/1+1/12	$\frac{2+n+D}{(1-D)}$	Low	$\frac{V_o}{2+n+D}$	$\frac{(1+n)V_o}{2+n+D}$	Yes	Low	96%
[23]	1/3/4/1+1/10	$\frac{n+1}{(1-D)}$	Low	$\frac{V_o}{n+1}$	$\frac{nV_o}{n+1}$	Yes	Very Low	95.6%
[24]	1/3/4/1+1/10	$\frac{n+2}{(1-D)}$	Low	$\frac{V_o}{n+2}$	$\frac{(1+n)V_o}{n+2}$	Yes	Very Low	95.7%
[25]	1/4/5/1+1/12	$\frac{1+n(1+D)}{(1-D)}$	Low	$\frac{V_o}{1+n(1+D)}$	$\frac{(1+n)V_o}{1+n(1+D)}$	Yes	Very Low	95.5%
[26]	1/4/5/1+1/12	$\frac{1+D+n(2-D)}{(1-D)}$	Low	$\frac{V_o}{1+D+n(2-D)}$	$\frac{(1+n)V_o}{1+D+n(2-D)}$	Yes	Very Low	96.7%
Proposed Converter	1/4/5/1+1/12	$\frac{2+n+nD}{(1-D)}$	Low	$\frac{V_o}{2+n+nD}$	$\frac{(1+n)V_o}{2+n+nD}$	Yes	Very Low	97.3%

S=Switch, D=Diode, C=Capacitor, CI =Coupled-Inductor, L=inductor, T=Total Device Count, Eff=Efficiency

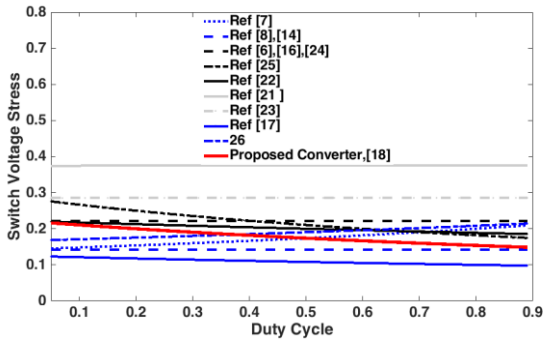


Fig. 11. Comparison of normalized voltage stress across main power switch of the converters given in Table *I* (*n* = 2.5).

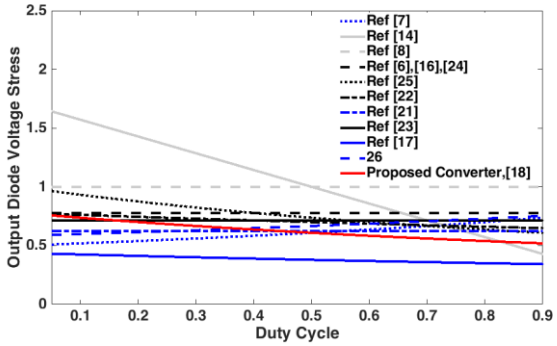


Fig. 12. Comparison of normalized voltage stress across output diode of the converters given in Table I (n = 2.5).

Using (18) and assuming 20% current ripple, the minimum value of L_{in} can be obtained as follows:

$$L_{in} > \frac{R_L.D}{20\%.M^2.f_s} \tag{38}$$

where f_s and R_L represent the switching frequency and the load As mentioned before the CI design is an important part of the converter analysis. The magnetizing inductor (L_M) of the CL can be designed by:

$$L_M > \frac{V_{Lm}.D}{\Delta I_{LM}.f_s} \tag{39}$$

where ΔI_{LM} is the allowable current ripple. Due to the placement of the magnetizing inductor in the middle of the proposed circuit, L_M can also be designed with a larger current ripple. The design of the CI with a smaller amount of L_m reduces the leakage inductance, core volume, and also the power losses. By substituting (14), (18), and (25) into (35), the minimum value of L_M is obtained as:

$$L_M > \frac{R_L.D}{\Delta\%.(n)M.f_s} \tag{40}$$

A. Capacitors

The proper value of converter capacitors can be determined based on their charge durations. The output capacitance is derived by using the following equation:

$$C_o = \frac{DV_{out}}{R_L.\Delta V_{Co}.f_s} \tag{41}$$

where ΔV_{Co} is the ripple present in the output DC voltage, which is usually acceptable to be 1% of the output DC voltage. The suitable values capacitors C_1, C_3, C_4 of the proposed converter can be determined as follows:

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTIE.2021.3074864, IEEE Journal of Emerging and Selected Topics in Industrial Electronics

$$C_1 = \frac{i_{LK}D}{\Delta V_{c1}.f_s} > \frac{M.D.n(1+\frac{\pi}{2D})}{\Delta\%.R_L.f_s} \quad (42)$$

$$C_3 = \frac{i_{D3}\mathrm{D}}{\Delta V_{c3}.f_s} > \frac{\pi.(1-D).M}{\Delta\%.2.(1+\mathrm{nD}).R_{LOAD}.f_s} \quad (43)$$

$$C_4 = \frac{i_{D3}\mathrm{D}}{\Delta V_{c4}.f_s} > \frac{\pi.(1-D).M}{\Delta\%.2.(1+\mathrm{n}).R_L.f_s} \quad (44)$$

where Δ% represents the allowable voltage ripple. Also, the design of the capacitor C_2 is based on its maximum current as:

$$C_2 = \frac{i_{D2}d_2}{\Delta V_{c2}.f_s} > \frac{2M(1-D)}{\Delta\%.n.D.R_O.f_s} \quad (45)$$

where, d_2 is the conduction time interval of the diode D_2, which is obtained as:

$$d_2 = \frac{2}{\mathrm{M+n}} \quad (46)$$

Furthermore, regarding (5) and operation analysis in Mode *III*, the QR duration is a function of the capacitors, C_1, C_3, and C_4. Consequently, the value of these capacitors is also selected from the following equation:

$$\pi\sqrt{L_{keq}[(n^2(C_3 \| C_4))\| C_1)]} = DT_S \quad (47)$$

It is necessary to mention that the middle capacitors of the proposed converter are not performing any filtering effect. Therefore, their design can be done under larger allowable voltage ripples. Thus, choosing small values for these capacitors will not affect the output voltage fluctuation. This will give the designer more freedom in selecting the capacitors. Consequently, the simplest and most effective way for adjusting the proposed converter resonant frequency is by properly selecting the values of the capacitors C_1 , C_3 and C_4 using the resonant frequency (47).

VI. Measurement Results

To justify the theoretical analysis of the QRHGHE-SEPIC, a 20 V to 200 V and 160 W (R_{Load}=250 Ω) output power prototype operating at a switching frequency 60 kHz is built in the laboratory as shown in Fig. 13. The specifications of the prototype are listed in Table *II*. Regarding the design considerations, the duty cycle and turns-ratio of the CL are chosen to be 0.55 and 1.84, respectively. Thanks to low voltage stress of the power switch, a low on-resistance MOSFET IRFP4110 with a very low ON resistance (i.e. 3.7 mΩ) is used for prototype implementation. The current and voltage waveforms were obtained using a high-frequency current probe PA-667 1MHZ and a differential probe GDP-025, respectivily.The steady state experimental waveforms are shown in Fig. 14-(i).

In Fig. 14 (a), the input inductor current in the time domain is presented, which is continuous with a low ripple (Δi_{Lin} = 1.5 A). From Fig. 14 (b), the main power switch turns on under ZCS condition with reduced turn-off current. Also, the voltage stress across the power switch is about V_{DS}=44 V. Thus, the power switch has a low power dissipation. From Fig. 15 and Fig.16 (a) the soft-switching status can be realized in the current shape of all diodes D_1, D_2, D_3 and D_o, which are summarized in Table III. Moreover, the peak reverse voltage across the diodes D_1, D_2, D_3 and D_o are 75 V, 40 V, 120 V and 120 V, respectively, which are much lower than the output voltage.

In addition, the output voltage along with the leakage inductor current are demonstrates in Fig. 16 (b). Due to the soft switching conditions of the output diode, the output voltage of the proposed converter is constant with a very small

Table II: DESIGN SPECIFICATIONS OF THE PROTOTYPE

Parameter	Values
Output Power(P_{out})	160 W
Input Voltage(V_{in})	20 V
Output Voltage(V_{out})	200 V
Switching Frequency(f_s)	60 kHz
Capacitors C_1	4.7 µF / 250 V
Capacitors C_2	47 µF / 100 V
Capacitors C_3	2.2 µF / 250 V
Capacitors C_4	6.6 µF / 160 V
Capacitor C_o	100 µF / 250 V
Power Switch	IRFP4110 / R_{DS}=3.7 mΩ
Input Inductors L_{in}	110 µH / T157-52
Magnetizing Inductor of the CL (L_m)	150 µH
Turns Ratio of the CL *n*	1.84 (19:35) / EE42/21/15
Merged Leakage Inductance L_K	2.3 µH
Diode D_1	SR3100 (V_F=0.85 V)
Diode D_2	SR360 (V_F=0.7 V)
Diode D_3	SR3150 (V_F=0.92 V)
Diode D_0	MUR420 (V_F=0.71 V)

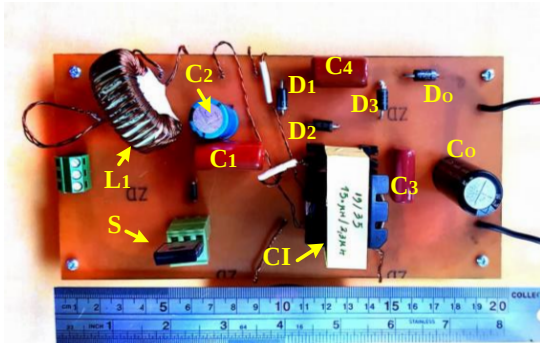
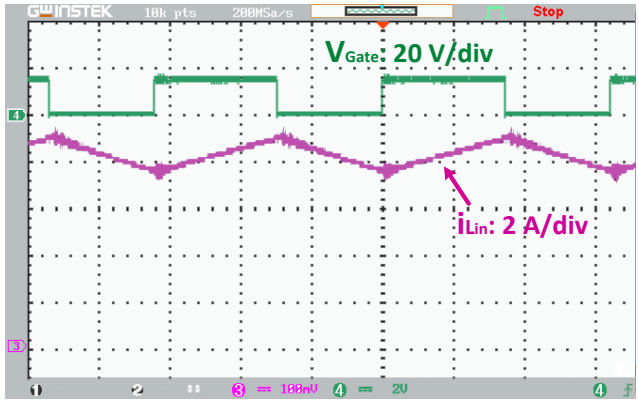
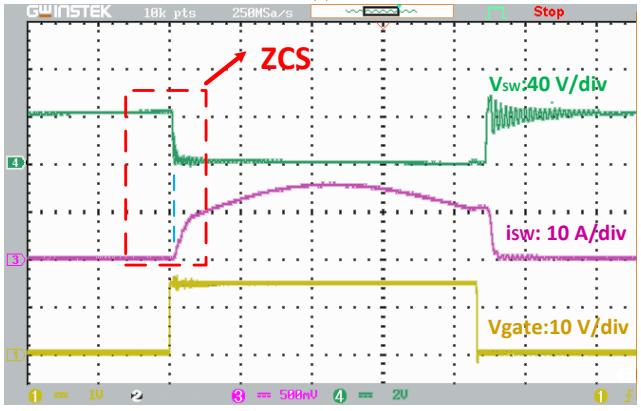


Fig. 13. Picture of the test setup and the experimental prototype.



(a)



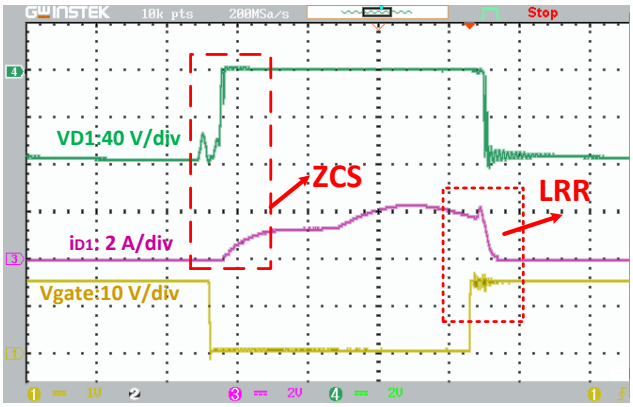
(b)

Fig. 14. Experimental results of the SSQBCI components. *(a) the input inductor (i_{Lin}), (b) the single power switch.*

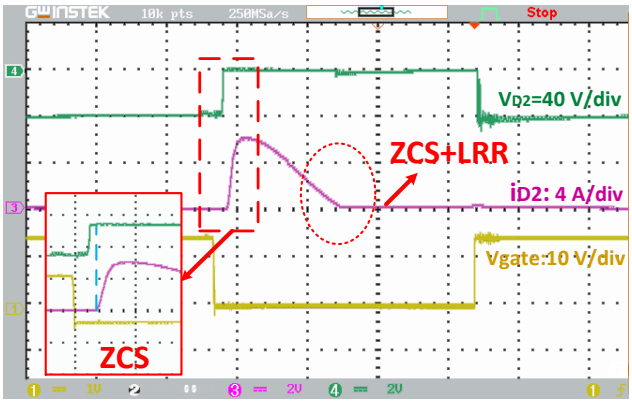
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTIE.2021.3074864, IEEE Journal of Emerging and Selected Topics in Industrial Electronics

voltage spike and noise at the switching instants.

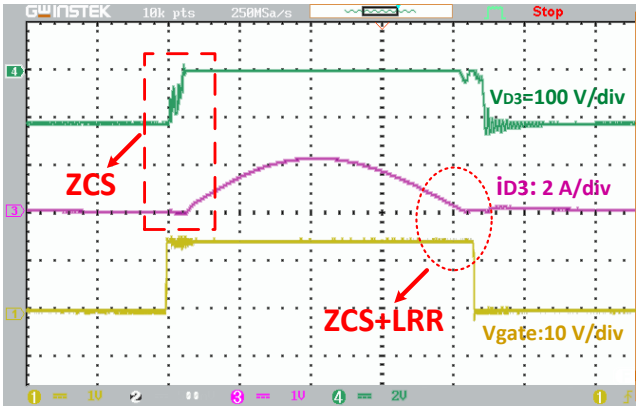
Moreover, the practical efficiency curve of the prototype versus output load levels from 30W to 160W and constant output voltage (V_o= 200 V) is plotted in Fig. 17. The efficiency is measured for two values of the input voltages V_{in}=20 V and V_{in}=30 V. The overall efficiency of the proposed converter at 20 V - 160 W operation is about 96.3%. As can be seen in this figure, increasing the input voltage source to 30 V, which leads to reduce the voltage gain from 10 to 6.6, can improve the converter efficiency.



(a)

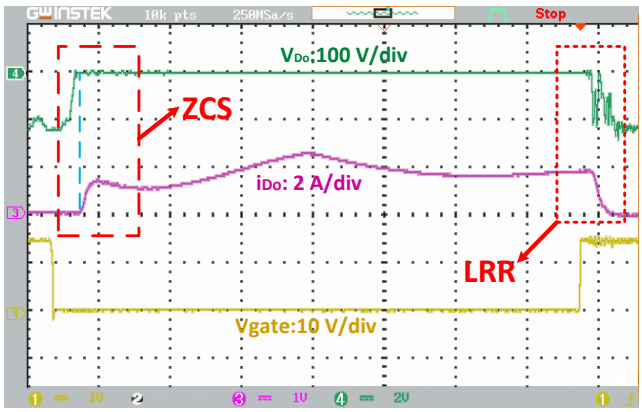


(b)

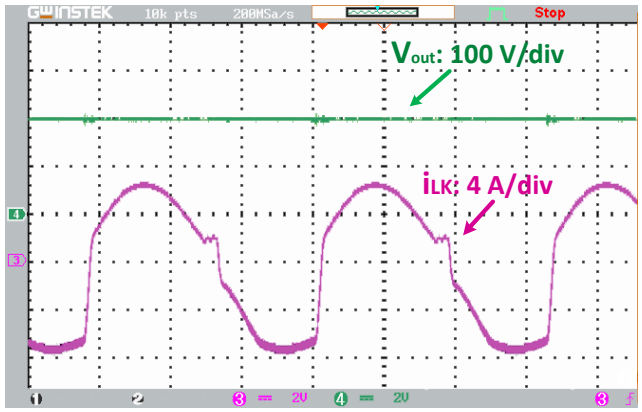


(c)

Fig. 15. Experimental results of the SSQBCI components. *(a) the diode D_1 , (b) the diode D_2 , (c) the diode D_3.*



(a)



(b)

Fig. 16. Experimental results of the SSQBCI components. *(a) the diode D_o , (b) the output voltage and the current of the leakage inductor of the CI.*

Table *III*: SOFT SWITCHING STATUS OF THE SWITCH AND THE DIODES OF THE PROPOSED CONVERTER.

Switching Device	**Soft –Switching Status**	
	Turn-on	***Turn-off***
D1	**ZCS**	**LRR**
D2	**ZCS**	**ZCS+LRR**
D3	**ZCS**	**ZCS+LRR**
Do	**ZCS**	**LRR**
MOSFET	**ZCS**	**With Low current**

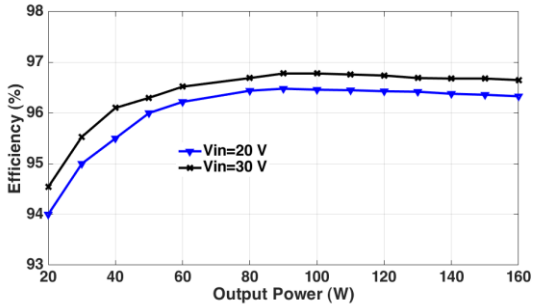


Fig. 17. Measured efficiency versus output powers.

The breakdown of power losses of the proposed converter at full load condition (V_{in} = 20 V, V_o = 200 V, and P_{out} = 160 W / R_L=250 Ω) is provided as a pie graph, which is illustrated in Fig. 18. This curve is calculated under the theoretical analysis provided in Section *III*. The Parasitic components (resistors and

forward drop voltage) are selected based on related datasheets for the proposed converter. Despite the high input current level, due to low voltage stress and soft-switching performance (i.e., ZCS and QR), the power dissipation portion of the power switch is lower than other losses. In addition, the verification plot of the experimental and theoretical voltage gain ratios from *D=0.3* to *D=0.75* is provided and is depicted in Fig. 19. Regarding this figure, in the critical mode, the proposed converter has the best performance.

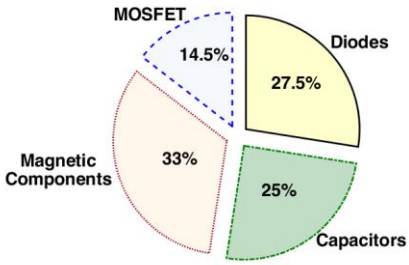


Fig. 18. Break-down of power losses at full load (V_{in} = 20 V, V_o = 200 V, and P_{out} = 160 W).

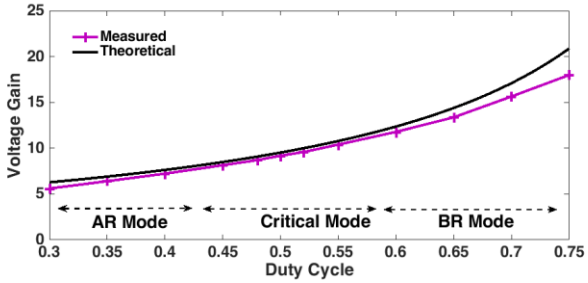
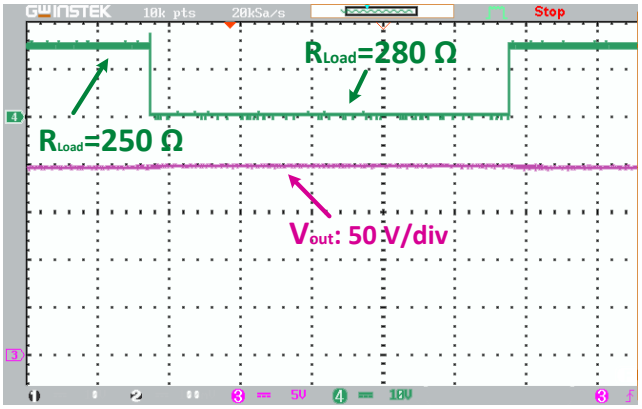


Fig. 19. The verification plot of the measured results and theatrical voltage gains.

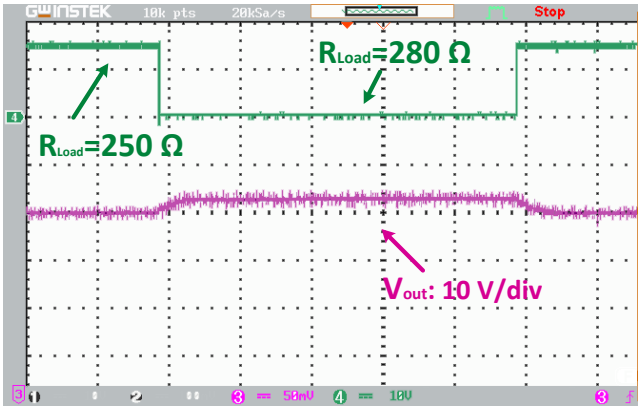
Finally, The hardware measurement of the dynamic response of the output voltage for a step change of 12% in the output load from R_L=250 Ω to R_L=280 Ω under V_{in}=20 V and V_{out}=200 V is provided and shown in Fig. 20, which proves the inherent stability of the proposed converter.

VII. Conclusion

A new single-switch SEPIC-based high step-up DC-DC converter is presented in this paper. High voltage gain, continuous input current with low ripple, low voltage spikes across the single power switch and diodes along soft-switching operation of all switching components are the traits of the proposed circuit. The steady-state analysis and design procedure have been presented in the CCM condition. The major performance indicators of the suggested converter have been compared with some other similar step-up converters and the merits of the QRHGHE-SEPIC have been justified. Experimental results from a 20 V-200 V /160 W laboratory prototype verified the validity of the design. The switching loss is significantly alleviated due to ZCS operation, which resulted



(a)



(b)

Fig.20. (a) The hardware measurement of the dynamic response of the output voltage for a 12% step change in the output load (R_L=250 Ωto R_L=280Ω), (b) the dynamic response of the output voltage with more details.

in high conversion efficiency. Considering the results of analysis and performances, the proposed QRHGHE-SEPIC can be a good candidate for small scale renewable energy applications.

References

[1] B. W. Williams, "DC-to-DC converters with continuous input and output power," *IEEE Trans. on Power Electron.*, vol. 28, DOI: 10.1109/TPEL.2012.2213272, no. 5, pp. 2307-2316, 2012.

[2] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of high-step-up coupled-inductor boost converters," *IEEE Journal of Emerging and Selected Topics in Power Electron.*, vol. 4, DOI: 10.1109/JESTPE.2016.2532930, no. 2, pp. 689-704, Feb. 2016.

[3] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: a comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. on Power Electron.*, vol. 32, DOI: 10.1109/TPEL.2017.2652318, no. 12, pp. 9143-9178, 2017.

[4] S. H. Hosseini and T. Nouri, "A transformerless step-up dc-dc converter with high voltage gain and reduced voltage stresses on semiconductors," in Conference UPEC, DOI: 10.1109/UPEC.2012.6398609, pp. 1-6, 2012.

[5] Q. Zhao and F. C. Lee, "High-efficiency, high step-up DC-DC converters," *IEEE Trans. on Power Electron.*, vol. 18, DOI: 10.1109/TPEL.2002.807188, no. 1, pp. 65-73, Mar. 2003.

[6] H. Ardi, A. Ajami, and M. Sabahi, "A novel high step-up DC–DC converter with continuous input current integrating coupled inductor for renewable energy applications," *IEEE Trans. on Industrial Electron*, vol. 65, DOI: 10.1109/TIE.2017.2733476, no. 2, pp. 1306-1315, 2017.

[7] L. He, Z. Zheng, and D. Guo, "High step-up DC–DC converter with active soft-switching and voltage-clamping for renewable energy systems," *IEEE*

Trans. on Power Electron., vol. 33, DOI: 10.1109/TPEL.2018.2789456, no. 11, pp. 9496-9505, 2018.

[8] N. Molavi, E. Adib, and H. Farzanehfard, "Soft-switched non-isolated high step-up DC–DC converter with reduced voltage stress," *IET Power Electron*., vol. 9, DOI: 10.1049/iet-pel.2015.0870, no. 8, pp. 1711-1718, 2016.

[9] K.-B. Park, G.-W. Moon, and M.-J. Youn, "Nonisolated high step-up stacked converter based on boost-integrated isolated converter," *IEEE Trans. on Power Electron*., vol. 26, DOI: 10.1109/TPEL.2010.2066578, no. 2, pp. 577-587, 2010.

[10] M. Heidari, H. Farzanehfard, and M. Esteki, "A Single-Switch Single-Magnetic Core High Conversion Ratio Converter With Low Input Current Ripple and Wide Soft-Switching Range for Photovoltaic Applications," *IEEE Trans. on Power Electron*., vol. 35, DOI: 10.1109/TPEL.2019.2958839, no. 7, pp. 7226-7234, 2019.

[11] H. Trazamni, E. Babaei, and M. Sabahi, "Full soft-switching high step-up DC–DC converter based on active resonant cell," *IET Power Electron.*, vol. 10, DOI: 10.1049/iet-pel.2016.1006, no. 13, pp. 1729-1739, 2017.

[12] W. Hassan, D. D.-C. Lu, and W. Xiao, "Analysis and experimental verification of a single-switch high-voltage gain ZCS DC–DC converter," *IET Power Electron*., vol. 12, DOI: 10.1049/iet-pel.2019.0076, no. 8, pp. 2146-2153, 2019.

[13] A. Ghasemi, S. F. Eilaghi, and E. Adib, "A new non-isolated high step-up SEPIC converter for photovoltaic applications," *in PEDSTC*, DOI: 10.1109/PEDSTC.2012.6183383, pp. 51-56. Apr. 2012.

[14] A. Abramovitz, J. Yao, and K. Smedley, "Derivation of a family of high step-up tapped inductor SEPIC converters," *Electronics Letters*, vol. 50, DOI: 10.1049/el.2014.2190, no. 22, pp. 1626-1628, 2014.

[15] A. Maroufkhani, D. KazemiKia, and K. Abbaszadeh, "A new single-switch soft-switched high-step up DC-DC converter based on magnetic coupling," *in Conference PEDSTC*, DOI: 10.1109/PEDSTC49159.2020.9088359, pp. 1-6, 2020.

[16] G. Somiruwan, L. Gunawardena, D. Nayanasiri, and Y. Li, "High-Step-Up Boost Converter Based on Coupled Inductor, Voltage Lift and Clamp Cells," *in Applied Power Electronics Conference (APEC)*, DOI: 10.1109/APEC.2019.8721926, pp. 2305-2310, 2019.

[17] M. E. Azizkandi, F. Sedaghati, H. Shayeghi, and F. Blaabjerg, "Two-and three-winding coupled-inductor-based high step-up DC–DC converters for sustainable energy applications," *IET Power Electron*., DOI: 10.1049/iet-pel.2019.0139, vol. 13, no. 1, pp. 144-156, 2019.

[18] A. E. Khosroshahi, A. M. Shotorbani, H. Dadashzadeh, A. Farakhor, and L. Wang, "A New Coupled Inductor-Based High Step-Up DC-DC Converter for PV Applications," *in Conference COMPEL*, DOI: 10.1109/COMPEL.2019.8769630, pp. 1-7, 2019.

[19] Y. Zheng, B. Brown, W. Xie, S. Li, and K. Smedley, "High Step-Up DC–DC Converter With Zero Voltage Switching and Low Input Current Ripple," *IEEE Trans. on Power Electron*., vol. 35, DOI: 10.1109/TPEL.2020.2968613, no. 9, pp. 9418-9431, 2020.

[20] P.-H. Tseng, J.-F. Chen, and Y.-P. Hsieh, "A novel active clamp high step-up DC-DC converter with coupled-inductor for fuel cell system," *in IFEEC*, DOI: 10.1109/IFEEC.2013.6687525, pp. 326-331, 2013.

[21] F. Sedaghati and S. Pourjafar, "Analysis and implementation of a boost DC–DC converter with high voltage gain and continuous input current," *IET Power Electron*., vol. 13, DOI: 10.1049/iet-pel.2019.0973, no. 4, pp. 798-807, 2019.

[22] R. Moradpour, H. Ardi, and A. Tavakoli, "Design and implementation of a new SEPIC-based high step-up DC/DC converter for renewable energy applications," *IEEE Trans. on Industrial Electron*., vol. 65, DOI: 10.1109/TIE.2017.2733421, no. 2, pp. 1290-1297, 2017.

[23] S. Pourjafar, F. Sedaghati, H. Shayeghi, and M. Maalandish, "High step-up DC–DC converter with coupled inductor suitable for renewable applications," *IET Power Electron*., vol. 12, DOI: 10.1049/iet-pel.2018.5414, no. 1, pp. 92-101, 2018.

[24] Y. Deng, Q. Rong, W. Li, Y. Zhao, J. Shi, and X. He, "Single-switch high step-up converters with built-in transformer voltage multiplier cell," *IEEE Trans. on Power Electron*., vol. 27, DOI: 10.1109/TPEL.2012.2183620, no. 8, pp. 3557-3567, Jan. 2012.

[25] M. Forouzesh, K. Yari, A. Baghramian, and S. Hasanpour, "Single-switch high step-up converter based on coupled inductor and switched capacitor techniques with quasi-resonant operation," *IET Power Electron.*, vol. 10, DOI: 10.1049/iet-pel.2015.0923, no. 2, pp. 240-250, 2017.

[26] S. Hasanpour, A. Baghramian, and H. Mojallali, "A modified SEPIC-based high step-up DC–DC converter with quasi-resonant operation for renewable energy applications," *IEEE Trans. on Industrial Electron.*, vol. 66, DOI: 10.1109/TIE.2018.2851952, no. 5, pp. 3539-3549, 2018.

[27] R. Gules, W. M. Dos Santos, F. A. Dos Reis, E. F. R. Romaneli, and A. A. Badin, "A modified SEPIC converter with high static gain for renewable applications," *IEEE Tran. on Power Electron*., vol. 29, DOI 10/1109/TPEL.2013.2296053, no.11, pp. 5860-5871, Dec. 2014.

[28] K. R. Babu, M. Ramteke, H. Suryawanshi, and K. R. Kothapalli, "High Gain Soft Switched DC-DC Converter for Renewable Applications," *in TPEC*, DOI: 10.1109/TPEC48276.2020.9042570, pp. 1-6, 2020.

[29] Nag, Soumya Shubhra, and Santanu Mishra. "Coupled inductor based high gain current-fed DC-DC bridge converters." *In 2015 IEEE Industry Applications Society Annual Meeting*, pp. 1-6. IEEE, 2015.