A High Step-Up DC–DC Converter With High Voltage Gain and Zero-Voltage Transition

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***Abstract*—This article presents a new high-step-up dc–dc converter. The proposed converter optimally integrates the coupled inductors, voltage multiplier cells, and series capacitor techniques to attain high voltage gain with low voltage stress. Moreover, in this configuration, the voltage multiplier circuit not only participates in increasing the voltage gain but also absorbs the leakage energy. In addition, zero-voltage switching and zero-current switching conditions are obtained for all switches and diodes, respectively. As a result, overall efficiency is improved. In this topology, the leakage inductance of the coupled inductors is used as a resonant inductor. Therefore, no additional magnetic core is needed. Furthermore, the ripple of the input current is reduced by using the interleaving technique. Also, this converter features automatic uniform current-sharing characteristics due to the charge balance of the blocking capacitors. The experimental results obtained from a prototype with 12 V input and 180 V output validate the theoretical analyses.**

***Index Terms*—Coupled inductors, high step-up converters, interleaved operation, soft switching, zero-voltage switching (ZVS).**

I. Introduction

ENERGY is one of the most critical and primary factors for continuing human life. In recent years, replacing fossil fuels with renewable energies, including solar and wind energy, has been widely welcomed [1]. For network connection applications, it is usually necessary to convert distributed resource output voltage to a higher voltage [2].

In theory, the conventional boost converter just by having close-to-one duty cycles can reach high output voltages. In practice, this increases the voltage stress across the semiconductors, increases input current ripple, and reduces efficiency. Hence, in recent decades, there has been extensive research on new topologies to provide higher voltage conversion ratios [3], [4].

In [5], the multilevel technique is proposed to increase the output voltage. This method increases the complexity and the cost. The research works in [6] and [7] introduced two or more boost converters in series or cascading. Although the voltage gain is effectively improved, the cost of the entire system increases.

Using the coupled inductors is another solution to improve the voltage gain of the converters. In this technique, the conversion ratio is increased by choosing a proper turn ratio for the coupled windings. However, in converters with coupled inductors, passive snubbers or active clamp circuits are required to absorb the energy stored in the leakage inductors [8], [9], [10], [11]. As a result, the circuits are complicated, and the efficiency is reduced.

The capacitors can work as voltage sources to obtain high voltage output in dc–dc converters. Two boost converters using switched-capacitor cells are provided in [12] and [13]. These converters include n switched-capacitor cells. Each cell consists of a capacitor, a diode, and two power switches. However, in these circuits, the number of semiconductor devices increases. Aggressive currents during charging and discharging capacitors, and the formation of a capacitive loop, are other disadvantages of these converters [14], [15].

In [16], the voltage multiplier cell (VMC) is proposed. This cell consists of diodes and capacitors. However, several cells are required to achieve high-voltage gains [17].

This article proposes a new high step-up converter to attain a high voltage gain. With the most benefits mentioned above and minimum problems, a conventional interleaved boost converter is integrated with a VMC, coupled inductors, and a series capacitor. In this integration by selecting the appropriate turns ratio of the coupled inductors, high voltage gain can be achieved without overincreasing the duty cycle. Also, semiconductor devices have low voltage stresses. In this topology, the voltage multiplier circuit not only participates in increasing the voltage gain but also absorbs the leakage energy. The zero-voltage switching (ZVS) condition is obtained for all switches, by using leakage inductance as a resonant inductor without any auxiliary switch and magnetic core. It can eliminate switching losses and diminish the electromagnetic interference problem.

The rest of this article is organized as follows. Section II analyzes the circuit configuration and operation principles. Section III exhibits the design consideration and converter performance analysis. Section IV discusses the experimental outcomes. Finally, Section V concludes this article.

II. Circuit Configuration and Operation Principles

Fig. 1(a) shows the circuit structure of the proposed converter. S_1 and S_2 are the main switches, D_0 is the output diode,

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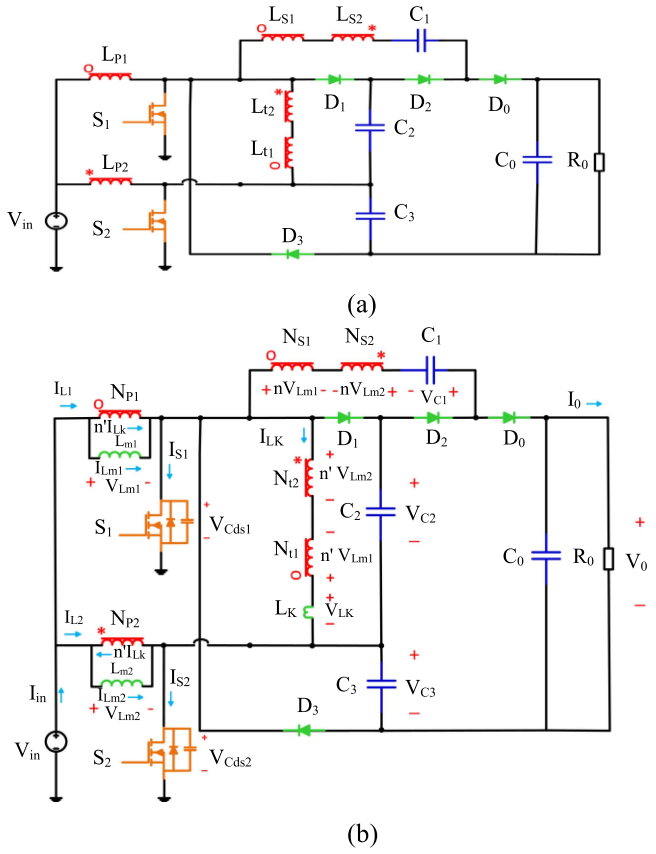

Fig. 1. Proposed converter. (a) Circuit structure. (b) Equivalent circuit.

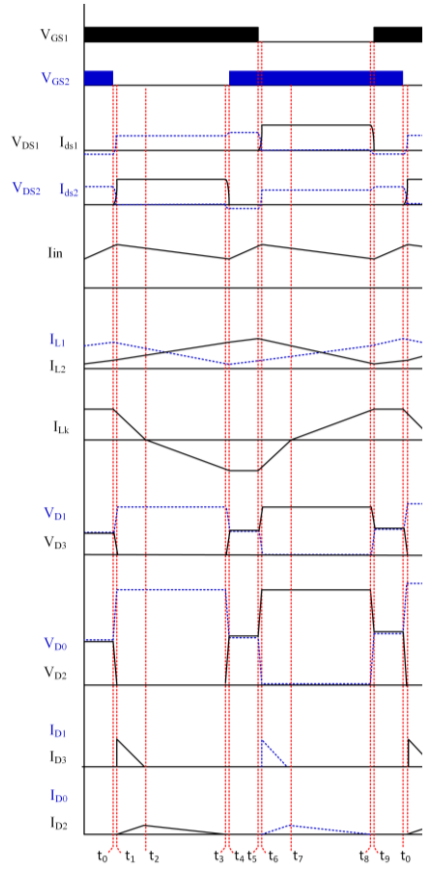

Fig. 2. Key waveforms of the proposed converter.

D_1, D_2, C_1, and C_2 make the VMC circuit, C_3 is the series capacitor, C_0 is the output capacitor, and R_0 is the load. Also, there are two cores with three windings. Fig. 1(b) shows the corresponding equivalent circuit of the proposed converter. The primary inductors L_{P1} and L_{p2} with N_p turns, respectively, are coupled with the secondary inductors L_{S1} and L_{S1} with N_s turns and the tertiary inductor L_{t1} and L_{t1} with N_t turns.

n and n' denote the N_S/N_P turns ratio and the N_t/N_p turns ratio, respectively. In this figure, the magnetizing inductances are represented with L_{m1} and L_{m2}. By reflecting leakage inductances from the primary and secondary of each phase to the tertiary side, L_K can be considered as the sum of them. C_{dS1} and C_{dS2} are the drain–source capacitors of S_1 and S_2.

The operating principles of the proposed converter are analyzed in this section. For analytical analyses, the following conditions are assumed.

1) The voltages of capacitors C_1, C_2, and C_3, which are represented by V_{C1}, V_{C2}, and V_{C3}, are assumed constant.
2) All converter components are ideal, except for the leakage inductance of the coupled inductors and the parasitic capacitors of the switches.
3) The current of the magnetizing inductor is considered constant.

Fig. 2 illustrates the theoretical waveforms, and Fig. 3 shows the equivalent circuits of the operating states. Operation states can be divided into ten states. Before the first state, S_1 and S_2 are ON.

State I [t_0–t_1]: At the beginning of this interval, the switch S_2 is turned OFF. All diodes are reverse-biased. Resonance occurs between the leakage inductor L_K and the capacitor of S_2. The current of L_K decreases, and the voltage of C_{ds2} increases resonantly. Therefore, ZVS turn-OFF is achieved for the switch S_2 [see Fig. 3(a)]

$$V_{Lm1} = V_{\text{in}} \tag{1}$$

$$V_{Lm2} = V_{\text{in}} - V_{Cds2} \tag{2}$$

$$I_{LK}(t) = A\cos(\omega(t-t_0)) + B\sin(\omega(t-t_0)) \tag{3}$$

$$A = i_{LK}(t_0),\ B = \frac{I_{LM}}{\sqrt{C_{ds2}L_K}},\ \omega = \frac{n'-1}{\sqrt{C_{ds2}L_K}} \tag{4}$$

$$I_{LK}(t) = i_{LK}(t_0)\cos\frac{n'-1}{\sqrt{C_{ds2}L_K}}(t-t_0) + \frac{I_{LM}}{\sqrt{C_{ds2}L_K}}\sin\frac{n'-1}{\sqrt{C_{ds2}L_K}}(t-t_0) \tag{5}$$

$$V_{Cds2}(t) = A\cos(\omega(t-t_0)) + B\sin(\omega(t-t_0)) \tag{6}$$

$$A = \frac{I_{LM}}{C_{ds2}}, B = -i_{LK}(t_0)\sqrt{\frac{L_K}{C_{ds2}}}, \omega = \frac{n'-1}{\sqrt{C_{ds2}L_K}} \tag{7}$$

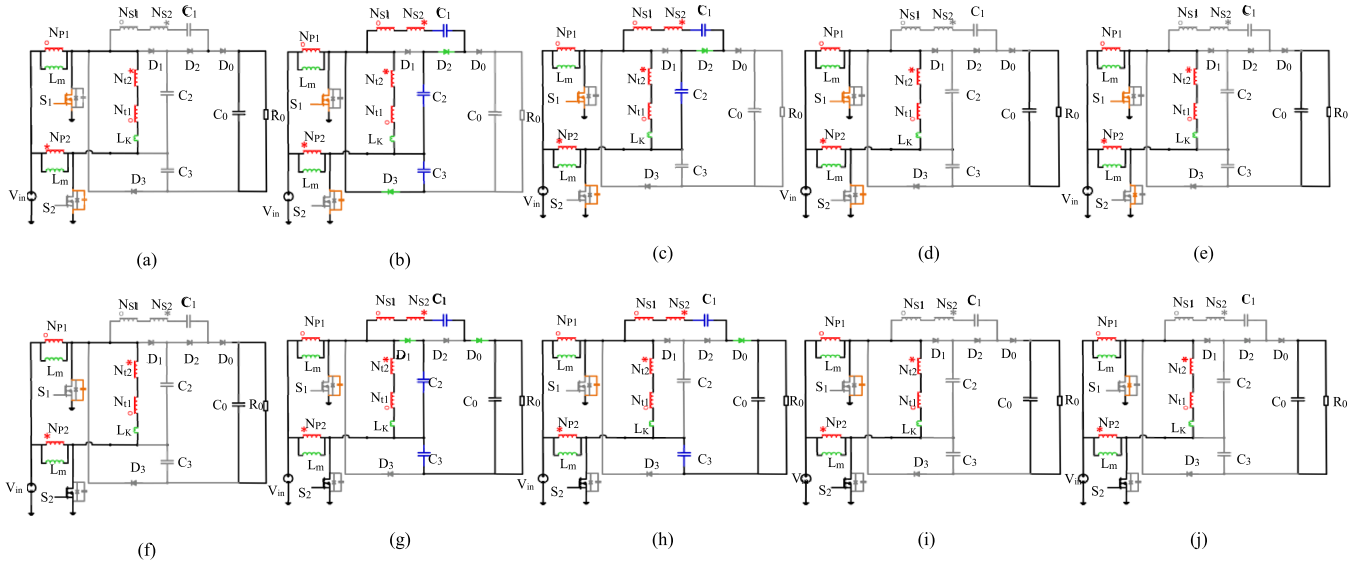

Fig. 3. Equivalent circuits of the operation modes. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII. (h) Mode VIII. (i) Mode IX. (j) Mode X.

$$V_{Cds2}(t) = \frac{I_{LM}}{C_{ds2}} \cos \frac{n'-1}{\sqrt{C_{ds2}L_K}}(t-t_0) - i_{LK}(t_0)\sqrt{\frac{L_K}{C_{ds2}}} \sin \frac{n'-1}{\sqrt{C_{ds2}L_K}}(t-t_0). \quad (8)$$

State II [t_1–t_2]: At t_1, the voltage of C_{ds2} reaches V_{C3}. The diodes D_2 and D_3 start to conduct. During this mode, I_{LK} decreases to zero linearly. The capacitors C_1 and C_3 charge and C_2 discharge [see Fig. 3(b)]

$$V_{Lm1} = V_{in} \quad (9)$$

$$V_{Lm2} = V_{in} - V_{Cds2} \quad (10)$$

$$V_{Cds2} = V_{C3} \quad (11)$$

$$I_{LK}(t) = \frac{(n'-1)V_{C3}}{L_k}(t-t_1) + I_{LK}(t_1). \quad (12)$$

State III [t_2–t_3]: This mode starts when I_{LK} and I_{D3} reach zero and diode D_3 turns OFF under the ZCS condition. In this state, the current of L_K increases linearly in the opposite direction [see Fig. 3(c)]

$$I_{LK}(t) = \frac{(n'-1)V_{C3}}{L_k}(t-t_2) + I_{LK}(t_2). \quad (13)$$

State IV [t_3–t_4]: At t_3, the current of D_2 reaches zero, and D_2 turns OFF under the ZCS condition. The capacitor C_{dS2} begins to discharge by the leakage inductor. At the end of this mode, the capacitor C_{dS2} is fully discharged [see Fig. 3(d)]. The related equations are given as follows:

$$V_{Lm1} = V_{in} \quad (14)$$

$$V_{Lm2} = V_{in} - V_{Cds2} \quad (15)$$

$$V_{Cds2} = V_{C3} \quad (16)$$

$$I_{LK}(t) = A\cos(\omega(t-t_3)) + B\sin(\omega(t-t_3)) \quad (17)$$

$$I_{LK}(t) = i_{LK}(t_3)\cos \frac{n'-1}{\sqrt{C_{ds2}L_K}}(t-t_3) + \left(\frac{I_{LM}}{\sqrt{C_{ds2}L_K}} + \sqrt{\frac{C_{ds2}}{L_K}}V_{C3}\right)\sin \frac{n'-1}{\sqrt{C_{ds2}L_K}}(t-t_3) \quad (18)$$

$$V_{Cds2}(t) = \left(\frac{I_{LM}}{C_{ds2}} + V_{C3}\right)\cos \frac{n'-1}{\sqrt{C_{ds2}L_K}}(t-t_3) - i_{LK}(t_3)\sqrt{\frac{L_K}{C_{ds2}}} \sin \frac{n'-1}{\sqrt{C_{ds2}L_K}}(t-t_3). \quad (19)$$

State V [t_4–t_5]: The antiparallel diode of S_2 begins to conduct at t_4. The voltage across S_2 is clamped to zero. Therefore, switch S_2 is turned ON under ZVS condition in this state. During this mode, the current of the leakage inductor is constant [see Fig. 3(e)].

State VI [t_5–t_6]: At t_5, switch S_1 is turned OFF. The drain–source capacitor of S_1 is charged through resonance with the leakage inductor L_K. Also, the current of L_K increases resonantly. As a result, switch S_1 is turned OFF under ZVS conditions [see Fig. 3(f)]. For this interval, the following equation is valid:

$$V_{Lm2} = V_{in} \quad (20)$$

$$V_{Lm1} = V_{in} - V_{Cds1} \quad (21)$$

$$I_{LK}(t) = A\cos(\omega(t-t_0)) + B\sin(\omega(t-t_0)) \quad (22)$$

$$A = i_{LK}(t_5),\ B = \frac{-I_{LM}}{\sqrt{C_{ds1}L_K}},\ \omega = \frac{n'-1}{\sqrt{C_{ds1}L_K}} \quad (23)$$

$$I_{LK}(t) = i_{LK}(t_5)\cos \frac{n'-1}{\sqrt{C_{ds1}L_K}}(t-t_5) - \frac{I_{LM}}{\sqrt{C_{ds1}L_K}} \sin \frac{n'-1}{\sqrt{C_{ds1}L_K}}(t-t_5) \quad (24)$$

$$V_{cds1}(t) = A\cos(\omega(t-t_5)) + B\sin(\omega(t-t_5)) \tag{25}$$

$$A = \frac{I_{LM}}{C_{ds1}},\ B = i_{LK}(t_5)\sqrt{\frac{L_K}{C_{ds1}}},\ \omega = \frac{n'-1}{\sqrt{C_{ds1}L_K}} \tag{26}$$

$$V_{cds1}(t) = \frac{I_{LM}}{C_{ds1}}\cos\frac{n'-1}{\sqrt{C_{ds1}L_K}}(t-t_5) + i_{LK}(t_5)\sqrt{\frac{L_K}{C_{ds1}}}\sin\frac{n'-1}{\sqrt{C_{ds1}L_K}}(t-t_5). \tag{27}$$

State VII [t_6–t_7]: At t_6, the voltage of S_1 reaches V_{C2}. The diodes D_0 and D_1 are turned ON, and the voltage of S_1 is clamped to V_{C2}. The current through D_2 reaches zero at the end of this state [see Fig. 3(g)]

$$V_{Lm2} = V_{\text{in}} \tag{28}$$

$$V_{Lm1} = V_{\text{in}} - V_{Cds1} \tag{29}$$

$$V_{Cds1} = V_{C2} \tag{30}$$

$$V_0 = V_{C1} + (n+1)V_{C2} + V_{C3} \tag{31}$$

$$I_{LK}(t) = \frac{(1-n')V_{C2}}{L_k}(t-t_6) + I_{LK}(t_6). \tag{32}$$

State VIII [t_7–t_8]: At the beginning of this state, I_{LK} and I_{D1} reach zero. The diode D_1 is turned OFF under ZCS conditions. During this mode, the leakage inductor current I_{LK} increases [see Fig. 3(h)]

$$V_{Cds1} = V_{C2} \tag{33}$$

$$I_{LK}(t) = \frac{(1-n')V_{C2}}{L_k}(t-t_7) + I_{LK}(t_7). \tag{34}$$

State IX [t_8–t_9]: At t_8, D_0 is naturally turned OFF with ZCS. The capacitor C_{dS1} discharges resonantly by the leakage inductor. At the end of this mode, these capacitors are fully discharged [see Fig. 3(i)]

$$V_{Lm2} = V_{\text{in}} \tag{35}$$

$$V_{Lm1} = V_{\text{in}} - V_{Cds1} \tag{36}$$

$$V_{Cds1} = V_{C2} \tag{37}$$

$$I_{LK}(t) = A\cos(\omega(t-t_8)) + B\sin(\omega(t-t_8)) \tag{38}$$

$$I_{LK}(t) = i_{LK}(t_8)\cos\frac{n'-1}{\sqrt{C_{ds1}L_K}}(t-t_8) - \left(\frac{I_{LM}}{\sqrt{C_{ds1}L_K}} + \sqrt{\frac{C_{ds1}}{L_K}}V_{C2}\right)\sin\frac{n'-1}{\sqrt{C_{ds1}L_K}}(t-t_8) \tag{39}$$

$$V_{Cds1}(t) = \left(\frac{I_{LM}}{C_{ds1}} + V_{C2}\right)\cos\frac{n'-1}{\sqrt{C_{ds1}L_K}}(t-t_8) + i_{LK}(t_8)\sqrt{\frac{L_K}{C_{ds1}}}\sin\frac{n'-1}{\sqrt{C_{ds1}L_K}}(t-t_8). \tag{40}$$

State X [t_9–t_0]: This mode starts when the voltage of capacitor C_{ds1} reaches zero. The antiparallel diode of switch S_1 begins to conduct. During this interval, the current of the leakage inductor is constant, and the S1 gate signal can be applied [see Fig. 3(j)].

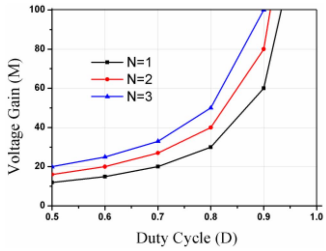

Fig. 4. Voltage gain versus duty cycle curves under different turns ratios.

III. Design Considerations and Converter Performance Analysis

A. Voltage Gain

The voltage gain is calculated by applying the volt–second balance principle on the magnetizing inductances L_{m1} and L_{m2}, which are as follows:

$$V_{\text{in}}DT_s = -(V_{\text{in}} - V_{C2})(1-D)T_s \tag{41}$$

$$V_{\text{in}}DT_s = -(V_{\text{in}} - V_{C3})(1-D)T_s. \tag{42}$$

Solving (41) and (42), the voltages of C_2 and C_3 are

$$V_{C2} = \frac{V_{in}}{(1-D)} = \frac{V_0}{(2n+4)} \tag{43}$$

$$V_{C3} = \frac{V_{\text{in}}}{(1-D)} = \frac{V_0}{(2n+4)}. \tag{44}$$

According to the Fig. 3(b), the following equation can be written:

$$V_{C1} = (n+1)V_{C3} + V_{C2}. \tag{45}$$

Substitute (43) and (44) into (45), the voltage of C_1 is derived as

$$V_{C1} = \frac{(n+2)V_{\text{in}}}{(1-D)} = \frac{(n+2)V_0}{(2n+4)}. \tag{46}$$

Based on (43)–(46) and Fig. 3(g), the voltage gain will be equal to

$$M = \frac{V_O}{V_{\text{in}}} = \frac{2n+4}{(1-D)}. \tag{47}$$

Fig. 4 shows the detailed plot of the voltage gain versus the duty cycle curves under different turn ratios.

By considering the leakage inductance effect and using the volt–second balance principle to magnetic inductances (L_{m1} and L_{m2}), the following equations are obtained:

$$V_{C3} = V_{C2} = \frac{L_m + n'^2 L_k}{L_m(1-D)}V_{\text{in}} \tag{48}$$

$$V_{C1} = \left(\frac{2\left(1 + n\frac{L_m}{\left(L_m + n'^2 L_k\right)}\right)}{\frac{L_m(1-D)}{\left(L_m + n'^2 L_k\right)}} + n\left(1 - \frac{L_m}{\left(L_m + n'^2 L_k\right)}\right)\right)V_{\text{in}}. \tag{49}$$

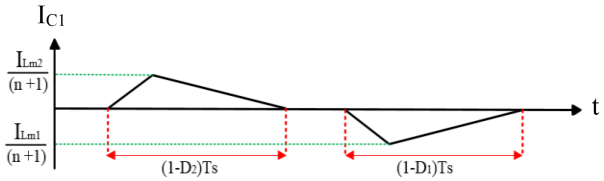

Fig. 5. Current waveform of C_1.

By applying the KVL principle on interval VII, the voltage gain is derived as

$$M = \frac{V_O}{V_{\text{in}}} = \frac{4(kn+1) - 2nk\,(D + k\,(1-D))}{k(1-D)} \tag{50}$$

where $k = \mathrm{L_m}/(\mathrm{L_m}+n^{'2}.\mathrm{L_k})$.

B. Voltage Stresses Across Semiconductor Devices

According to modes II and VII, the voltage stresses of the main switches S_1 and S_2 are

$$V_{S2,\max} = V_{C3} = \frac{V_0}{(2n+4)} \tag{51}$$

$$V_{S1,\max} = V_{C2} = \frac{V_0}{(2n+4)}. \tag{52}$$

According to modes III and VIII, the voltage stresses on the diodes obtained as

$$V_{D0} = V_{D2} = \frac{2(n+1)V_{\text{in}}}{(1-D)} = \frac{(n+1)V_0}{(n+2)} \tag{53}$$

$$V_{D1} = V_{D3} = \frac{2V_{\text{in}}}{(1-D)} = \frac{V_0}{(n+2)}. \tag{54}$$

C. Automatic Uniform Current Sharing

By ignoring the first, fourth, sixth, and ninth intervals, due to their small durations, the current waveform of blocking capacitor C_1 is shown in Fig. 5. By using the ampere–second balance principle for C_1, the following equation has to be satisfied:

$$\frac{I_{Lm2}}{2(n+1)} \cdot (1-D)T_s = \frac{I_{Lm1}}{2(n+1)} \cdot (1-D)T_s. \tag{55}$$

According to the above equation, in equal duty cycles, $\mathrm{I_{Lm1}}$ is similar to $\mathrm{I_{Lm2}}$. Therefore, automatic uniform current sharing is provided in this topology.

D. Soft-Switching Condition

This proposed converter provided ZVS soft switching performance for both switches, which improves conversion efficiency by reducing power losses in the switch. At the turn-OFF instant, the drain–source capacitors of the switches $\mathrm{C_{ds1}}$ and $\mathrm{C_{ds2}}$ limit the rate of the switch's voltage change; thus, the ZVS turn-OFF of the switches is achieved. The resonance between the leakage inductance and the drain–source capacitors causes these capacitors to discharge resonantly, so the anti-parallel diodes conduct and the switches are turned ON under ZVS conditions. To ensure ZVS is turned ON for the switches, the drain–source capacitors must be discharged entirely by leakage inductance during modes IV and IX. Therefore, the following equation must be satisfied:

$$\frac{1}{2}L_{LK}.(I_{LK}\,(t_3))^2 \geq \frac{1}{2}C_{DS}.(V_{C_{\text{DC}}}\,(t_3))^2 \tag{56}$$

where $C_{DS} = C_{\mathrm{ds1}} = C_{\mathrm{ds2}}$.

E. Comparison

Table I compares the introduced topology and recent high-voltage gain topologies with coupled inductors. By substituting the same duty cycle and the turns ratio into the voltage gain formulas, it can be observed that the voltage gain of the proposed converter is remarkably improved. This improvement will become more evident in high turn ratios. Moreover, the ZVS condition is provided for all switches at turn-ON and turn-OFF instants, which reduces switching loss and improves efficiency. In addition, the ZCS conditions are obtained for all diodes. Unlike the converters presented in [20], the proposed topology provides the above soft switching condition without any additional magnetic core and the additional switch. In the proposed topology, the leakage inductance controls the current falling rates of diodes, so the diode reverse-recovery problem is diminished. Furthermore, because of the uniform current-sharing characteristic of the proposed converter, the large input current is shared between the two interleaved phases. The maximum theoretical efficiency for the proposed converter is given in this table.

F. Loss Analysis

In this section, power loss is theoretically analyzed. The total power losses mainly contain four parts given by

$$P_{\text{Losses}} = P_S + P_D + P_C + P_L \tag{57}$$

where P_S is the switches loss, P_D is the diodes loss, P_L is the coupled inductors loss, and P_C is the loss of capacitor.

Switch loss is equal to the sum of switching ($P_{S(\text{switching})}$) and conduction losses ($P_{S(\text{ON})}$). In the converter proposed in this article, due to the ZVS operation of the switches, the switching loss is approximately zero. The switching and conduction losses of switches are

$$\begin{aligned} P_{(\text{Switching})} &= P_{\text{SW1}} + P_{\text{SW2}} \\ &= \frac{f_s}{2}\left(V_{ds_1} I_{L_1} t_{\text{OFF1}} + V_{ds2} I_{L2} t_{\text{OFF2}}\right) \\ P_{S_1} &= r_{ds_1}.I^2_{S_1(\text{rms})} \\ &= r_{ds_1}\frac{I_{Lm}}{(1-n')}\sqrt{(1-D)\left(\frac{1-n'}{1+n}+1\right)} \end{aligned} \tag{58}$$

$$\begin{aligned} P_{S2} &= r_{ds_2}.I^2_{S_2(\text{rms})} \\ &= r_{ds_2}\frac{I_{Lm}}{(1-n')}\sqrt{(1-D)\left(\frac{1-n'}{1+n}+1\right)} \end{aligned} \tag{59}$$

where r_{ds} is the power switch ON-state resistance and t_{OFF} is the time interval for the MOSFETs to be turned OFF.

TABLE I
COMPARISON RESULTS AMONG SOME CONVERTERS, CONVENTIONAL CONVERTER, AND PROPOSED CONVERTER

	Proposed converter	[21]	[18]	[20]	[19]	[22]	[23]
Voltage gain	$\frac{2n+4}{1-D}$	$\frac{3n+2}{1-D}$	$\frac{2n+4}{1-D}$	$\frac{2n+2}{1-D}$	$\frac{1}{(1-D)2}$	$\frac{3+2n-D(3+n-D)}{(1-D)2}$	$\frac{(N+1)}{1-D}$
The maximum voltage stress on main switches	$\frac{V_0}{(2n+4)}$	$\frac{V_0}{(3n+2)}$	$\frac{V_0}{(2n+4)}$	$\frac{V_0}{(2n+2)}$	$\frac{V_0(4-2D)}{1-D}$	$\frac{V_0}{3+2n-D(3+n-D)}$	V_0
Voltage stress of output diode (D_0)	$\frac{V_0(n+1)}{(n+2)}$	$\frac{V_0(2n+1)}{(3n+2)}$	$\frac{V_0(n+1)}{(n+2)}$	V_0	-	$\frac{nV_0(2-D)}{3+2n-D(3+n-D)}$	V_0
Input current ripple (%)	$\frac{R_o(2D-1)(1-D)^2}{4Lf_S.(n+2)^2}$	$\frac{R_o(2D-1)(1-D)^2}{Lf_S.(3n+2)^2}$	$\frac{R_o(2D-1)(1-D)^2}{4Lf_S.(n+2)^2}$	$\frac{R_o(2D-1)(1-D)^2}{4Lf_S.(n+1)^2}$	$\frac{R_o(2D-1)(1-D)^2}{4Lf_S.(n+2)^2}$	High-118%	$\frac{R_oD(1-D)^2}{Lf_S.(n+1)^2}$
V_{in}(V)/V_{out}(V)	12/180	30/400	40/580	48/380	24/110	30/400	30/400
f_S(kHz)	100	50	40	50	40	50	100
Blocking capacitor values (μF)	6.8,22,22,56	30,30,10 4.7,4.7,4.7	10,10,220,470	9,3,120	470,470, 470	180,180,22,22,22	2.2,470
Magnetizing inductance values (μH)	100,100	364	700,700	720,720,300	200	100,200	600
Number of switches	2	2	2	4	4	2	1
Number of diodes	4	8	4	2	0	5	2
Number of magnetic cores	2	2	3	3	1	2	1
Number of windings	6	6	4	4	2	3	2
Number of capacitors	4	6	4	3	3	5	2
Soft switching of switches	ZVS	-	ZCS	ZVS	-	-	-
Efficiency	97.1	97%	95.3%	97.76%	90%	96.3%	97%

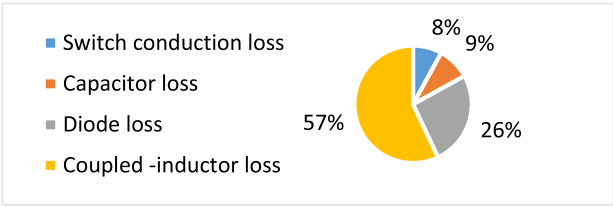

Fig. 6. Theoretical analysis of power loss distribution at rated power.

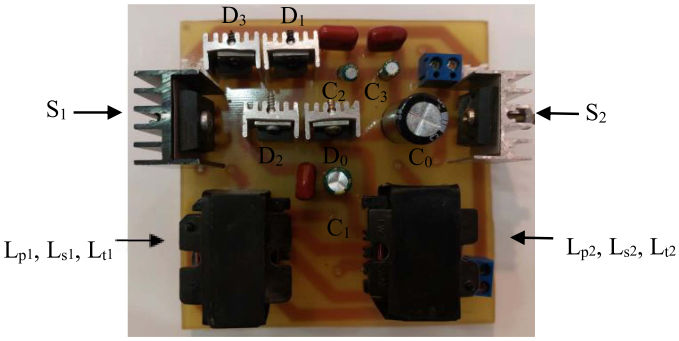

Fig. 7. Picture of the prototype.

The conduction losses for diodes D_1, D_2, D_3, and D_0 can be calculated as

$$P_{D_{0,1,2,3}} = V_{F_{0,1,2,3}} \cdot I_{D_{0,1,2,3}(\text{avg})} = V_{F_{0,1,2,3}} \cdot I_0. \quad (60)$$

where V_F is the forward voltage drop of diodes.

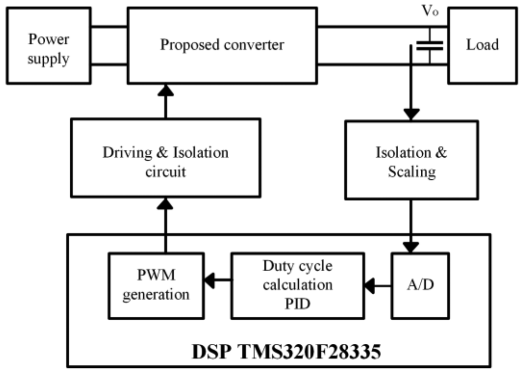

Fig. 8. The control diagram.

The conduction losses in capacitors can be obtained as

$$P_{C_1} = R_{\text{ESR}_1}.I^2_{C_1(\text{rms})} = R_{\text{ESR}_1}\frac{I_{Lm}}{n+1}\sqrt{\frac{4(1-D)}{3}+\frac{2(1-D)^2}{1-D-D_a}} \quad (61)$$

$$P_{C_2} = P_{C_3} = R_{\text{ESR2,3}}.I^2_{C_2(rms)} = R_{\text{ESR2,3}}I_{Lm}\sqrt{\frac{(1-D)(1-D+2D_a)}{3(n+1)^2(1-D-D_a)}+\frac{D_a}{3(1-n')^2}} \quad (62)$$

where $D_a = \frac{(1-n')(1-D)}{(1+n)}$, and $\text{R}_{\text{ESR1,2,3}}$ is the equivalent series resistance of the capacitors.

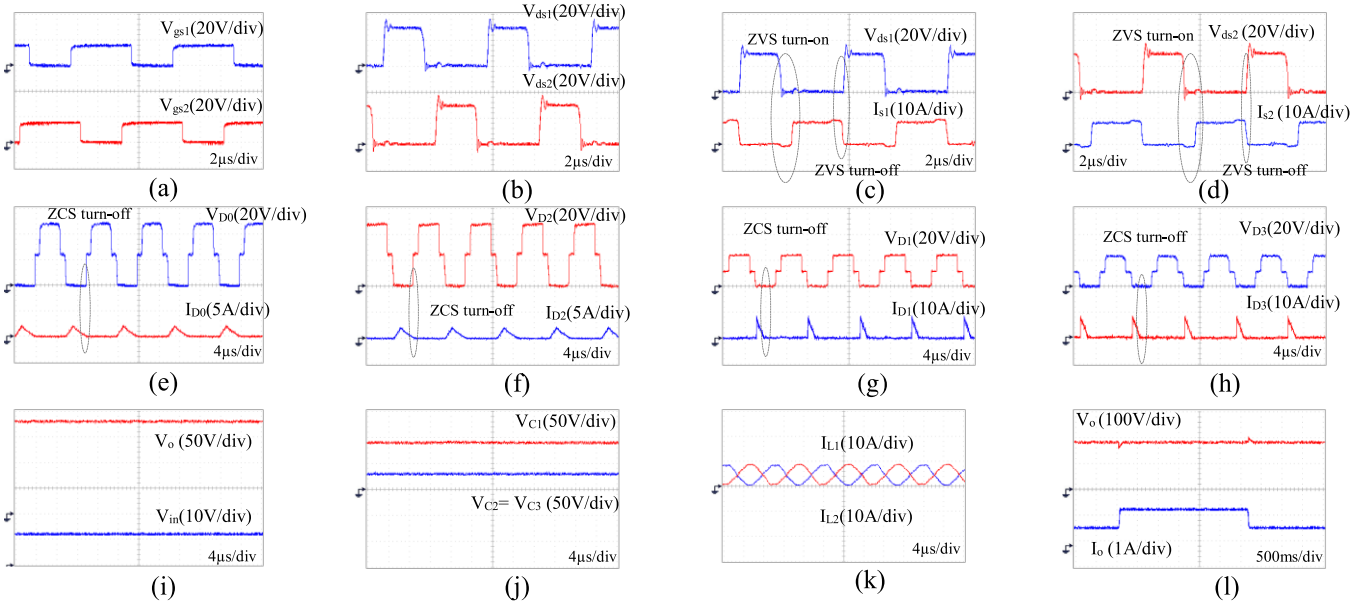

Fig. 9. Experimental results of the proposed converter.

Total power losses of the coupled inductors are

$$P_L = P_{\text{Cond}} + P_{\text{Core}}.$$

The core loss has been calculated according to the improved generalized Steinmetz equation method in [24].

By assuming r_{Lp}, r_{Ls}, and r_{Lt} are the primary-side, secondary-side, and tertiary-side windings resistance of the inductors, respectively. The total coupled inductor loss is calculated as

$$P_{L-\text{Cond}} = r_{Lp_1} I^2_{Lp1,\text{rms}} + r_{Lp_2} I^2_{Lp2,\text{rms}} + \left(r_{Ls_1} + r_{Ls_2}\right) I^2_{Ls,\text{rms}} + \left(r_{Lt_1} + r_{Lt_2}\right) I^2_{Lt,\text{rms}} \tag{63}$$

where

$$I_{Lp1,\text{rms}} = I_{Lp2,\text{rms}} = I_{Lp,\text{rms}} \tag{64}$$

$$I_{LS,\text{rms}} = I_{D2,\text{rms}} = \frac{I_{Lm}}{n+1}\sqrt{\frac{2\,(1-D)}{3} + \frac{(1-D)^2}{1-D-D_a}} \tag{65}$$

$$I_{Lt,\text{rms}} = I_{Lk,\text{rms}} = \frac{I_{Lm}}{(1-n')} \times \sqrt{2\left(\frac{(1-D)^2 + 2(1-D-D_a)^2}{(1-D-D_a)}\right) + \frac{14\,(1-D)}{3} + 1.} \tag{66}$$

Based on the selected components for a prototype, the losses of each component are shown in Fig. 6.

G. Design of Capacitors and Magnetizing Inductors

Assuming that the voltage ripple of each capacitor is $r\%$ of the maximum voltage value of the capacitor ($\Delta V_C = r\%.V_C$), their values can be determined as follows:

$$C_0 = \frac{I_0}{\Delta V_{C0} \cdot f_S} = \frac{I_0\,(1-D)}{r\%\,(2n+4) \cdot V_{\text{in}} \cdot f_S} \tag{67}$$

$$C_1 = \frac{I_0}{\Delta V_{C1} \cdot f_S} = \frac{I_0\,(1-D)}{r\%\,(n+2) \cdot V_{\text{in}} \cdot f_S} \tag{68}$$

$$C_2 = C_3 = \frac{I_0}{\Delta V_{C2} \cdot f_S} = \frac{I_0\,(1-D)}{r\% \cdot V_{\text{in}} \cdot f_S} \tag{69}$$

where ΔV_C and f_S are considered as the voltage ripple of capacitors and switching frequency, respectively.

To choose the proper magnetizing inductors, relying on the current ripple of each magnetizing inductor ($\Delta I_{Lm} = x\%.I_{Lm}$), the minimum value of L_m could be derived

$$L_m = L_{m1} = L_{m2} = \frac{V_{\text{in}} \cdot D}{\chi\% \cdot I_{Lm} \cdot f_S} = \frac{2 \cdot V_{\text{in}} \cdot D}{\chi\% \cdot I_{\text{in}} \cdot f_S} = \frac{V_{\text{in}} \cdot D\,(1-D)}{\chi\% \cdot (n+2)\,I_o \cdot f_S}. \tag{70}$$

IV. Experimental Results

To validate the theoretical results, a prototype is built based on Table II. Fig. 7 presents a picture of the prototype, and the control diagram is plotted in Fig. 8.

The experimental waveforms of the proposed converter are shown in Fig. 9. As can be seen in Fig. 9(a), the gate signals are interleaved to reduce the current ripple. The drain-to-source voltages of the switches are shown in Fig. 9(b). As can be observed, the voltage stresses of the switches are clamped at 30 V, which matches the calculation from (51) and (52). The

TABLE II
CIRCUIT PARAMETERS

Components	Parameters
Output power (P_o)	100 W
Input/output voltages (V_{in} /V_o)	12 V/180 V
Switching frequency (f_S)	100 kHz
Power MOSFETs (S_1 and S_2)	IRF100P219
Diodes (D_0, D_1, D_2 and D_3)	BYC 10 600
Capacitors (C_0, C_1, C_2 and C_3)	56 μF, 6.8 μF, 22 μF, 22 μF (parallel with 100 nF film capacitor)
Coupled inductors	Turns ratio (N_P:N_S) = 1:1, Turns ratio (N_P:N_t)= 2:1 Magnetizing inductance L_m = 100 μH Leakage inductance = 3.6 μH

current and voltage waveforms of switches S_1 and S_2 are plotted in Fig. 9(c) and (d), respectively. It is clear that ZVS condition has been provided for all switches in turn-OFF mode, and also they are turned ON under ZVS condition. Fig. 9(e) and (f) shows the voltages and currents across the diode D_0 and D_2, respectively. The blocking voltages of D_0 and D_2 are around 120 V, which matches the calculations from (53). Also, these diodes are turned OFF naturally under ZCS. Fig. 9(g) and (h) show the voltages and currents across the diode D_1 and D_3, respectively. The blocking voltages of D_1 and D_3 are around 60 V, which matches the calculations from (54). Also, these diodes are turned OFF naturally under ZCS, and the reverse recovery currents of the diodes are alleviated. Fig. 9(i) shows the input and output voltage when the turns ratio is 1. As can be observed in Fig. 9(j), the voltages of C_1 and C_2 (V_{C1} and V_{C2}) are around 90 and 30 V, which are consistent with the calculations from (46) and (43). According to calculations (43) and (44), V_{C3} equals V_{C2}. Fig. 9(j) confirms this equality. Fig. 9(k) gives the current of the primary inductors L_{p1} and L_{p2}. The large input current is shared between the two interleaved phases due to the uniform current-sharing characteristic of the converter. The dynamic response of the proposed converter for the load change between half load and full load is shown in Fig. 9(l).

V. CONCLUSION

This article presented an efficient interleaved high-step-up dc–dc converter. All semiconductor devices operated at soft-switching conditions without utilizing any auxiliary switch and magnetic core by employing leakage inductance as a resonant inductor. Moreover, the leakage inductance controlled the current falling rate of the diodes, which alleviated the diode reverse recovery problem. By using coupled inductors, a high voltage gain was achieved. VMC in the proposed converter recycled the leakage energy and clamped the voltage stress on the switches in addition to increasing the output voltage. Therefore, the voltage stresses on switches were low. Utilizing low-voltage-rating switches with small ON-resistances reduced the conduction losses. In addition, this converter showed automatic current-sharing characteristics. To verify the validity of the theoretical analysis, a 12 V/180 V laboratory prototype of this converter was built, and its results were investigated.

REFERENCES

[1] S. M. Amin and B. F. Wollenberg, "Toward a smart grid: Power delivery for the 21st century," *IEEE Power Energy Mag.*, vol. 3, no. 5, pp. 34–41, Sep./Oct. 2005, doi: 10.1109/MPAE.2005.1507024.

[2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004, doi: 10.1109/TPEL.2004.833453.

[3] T. G. Wilson, "The evolution of power electronics," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 439–446, May 2000, doi: 10.1109/63.844503.

[4] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011, doi: 10.1109/TIE.2010.2049715.

[5] A. Shoaei, K. Abbaszadeh, and H. Allahyari, "A single-inductor multi-input multilevel high step-up DC–DC converter based on switched-diode-capacitor cells for PV applications," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 4, no. 1, pp. 18–27, Jan. 2023, doi: 10.1109/JESTIE.2022.3173178.

[6] S.-W. Lee and H.-L. Do, "High step-up coupled-inductor cascade boost DC–DC converter with lossless passive snubber," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7753–7761, Oct. 2018, doi: 10.1109/TIE.2018.2803731.

[7] X. Hu, X. Liu, Y. Zhang, Z. Yu, and S. Jiang, "A hybrid cascaded high step-up DC–DC converter with ultralow voltage stress," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1824–1836, Apr. 2021, doi: 10.1109/JESTPE.2020.2975856.

[8] A. Asghari, "Ultra-high step-down ZVS synchronous buck converter with low switch voltage stress," *Int. Eng. Technol. Power Electron.*, vol. 13, no. 10, pp. 2039–2048, 2020, doi: 10.1049/iet-pel.2019.1113.

[9] T. Liu, M. Lin, and J. Ai, "High step-up interleaved DC–DC converter with asymmetric voltage multiplier cell and coupled inductor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4209–4222, Dec. 2020, doi: 10.1109/JESTPE.2019.2931634.

[10] P. Talebi and H. Farzanehfard, "Fully soft switched coupled inductor-based high step-up converter with active clamp and low switch voltage stress," in *Proc. 13th Power Electron., Drive Syst., Technol. Conf.*, 2022, pp. 281–286, doi: 10.1109/PEDSTC53976.2022.9767240.

[11] A. Asghari, "A soft switching four-phase converter with ultra-high step down conversion ratio and automatic uniform current sharing," *Int. Eng. Technol. Power Electron.*, vol. 14, no. 10, pp. 1489–1503, 2021, doi: 10.1049/pel2.12126.

[12] M. Zhang, Z. Wei, M. Zhou, F. Wang, Y. Cao, and L. Quan, "A high step-up DC–DC converter with switched-capacitor and coupled-inductor techniques," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 3, no. 4, pp. 1067–1076, Oct. 2022, doi: 10.1109/JESTIE.2022.3173909.

[13] R. Rahimi, S. Habibi, M. Ferdowsi, and P. Shamsi, "An interleaved high step-up DC-DC converter based on integration of coupled inductor and built-in-transformer with switched-capacitor cells for renewable energy applications," *IEEE Access*, vol. 10, pp. 34–45, 2022, doi: 10.1109/ACCESS.2021.3138390.

[14] S.-W. Seo, J.-H. Ryu, Y. Kim, and H. H. Choi, "Non-isolated high step-up DC/DC converter with coupled inductor and switched capacitor," *IEEE Access*, vol. 8, pp. 217108–217122, 2020, doi: 10.1109/ACCESS.2020.3041738.

[15] C. Cui, Y. Tang, Y. Guo, H. Sun, and L. Jiang, "High step-up switched-capacitor active switched-inductor converter with self-voltage balancing and low stress," *IEEE Trans. Ind. Electron.*, vol. 69, no. 10, pp. 10112–10128, Oct. 2022, doi: 10.1109/TIE.2021.3135611.

[16] X. Liu, X. Zhang, X. Hu, H. Chen, L. Chen, and Y. Zhang, "Interleaved high step-up converter with coupled inductor and voltage multiplier for renewable energy system," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 4, pp. 299–309, Dec. 2019, doi: 10.24295/CPSSTPEA.2019.00028.

[17] T. Nouri, N. V. Kurdkandi, and M. Shaneh, "A novel ZVS high-step-up converter with built-in transformer voltage multiplier cell," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12871–12886, Dec. 2020, doi: 10.1109/TPEL.2020.2995662.

[18] T. Nouri, N. V. Kurdkandi, and M. Shaneh, "A novel interleaved high step-up converter with built-in transformer voltage multiplier cell," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4988–4999, Jun. 2021, doi: 10.1109/TIE.2020.2992944.

[19] A. R. N. Akhormeh, K. Abbaszadeh, M. Moradzadeh, and A. Shahirinia, "High-gain bidirectional quadratic DC–DC converter based on coupled inductor with current ripple reduction capability," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 7826–7837, Sep. 2021, doi: 10.1109/TIE.2020.3013551.

[20] S. H. Ghaffarpour, S. E. Afjei, and A. Salemnia, "A novel soft-switched interleaved high step-up DC–DC converter for high-efficiency conversion," *Int. J. Circuit Theory Appl.*, vol. 49, pp. 2515–2532, 2021.

[21] J. Semiromizadeh, H. Izadi, and E. Adib, "High step-up interleaved DC-DC converter for photovoltaic systems," *Int. Eng. Technol. Power Electron.*, vol. 15, no. 1, pp. 33–42, 2022.

[22] M. Rezaie and V. Abbasi, "Ultrahigh step-up DC–DC converter composed of two stages boost converter, coupled inductor, and multiplier cell," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 5867–5878, Jun. 2022, doi: 10.1109/TIE.2021.3091916.

[23] R. Afzal, Y. Tang, H. Tong, and Y. Guo, "A high step-up integrated coupled inductor-capacitor DC-DC converter," *IEEE Access*, vol. 9, pp. 11080–11090, 2021, doi: 10.1109/ACCESS.2020.3048354.

[24] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Improved core-loss calculation for magnetic components employed in power electronic systems," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 964–973, Feb. 2012, doi: 10.1109/TPEL.2011.2162252.

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