# A Virtual Inertia and Damping Control to Suppress Voltage Oscillation in Islanded DC Microgrid

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Abstract—In this paper, a virtual inertia and damping control (VIDC) strategy is proposed to enable bidirectional DC (bi-DC) converter to dampen the voltage oscillation, using the energy stored in energy storage system (ESS) to emulate the inertia of DC microgrid (DC-MG) without modifications of system hardware. Both inertia part and damping part are modelled in the VIDC regulator, by analogizing with DC machine. Droop control is introduced to achieve multi-parallel operation of ESS. Further, its small signal model is established and the dynamic characteristic of the DC bus voltage during power fluctuation is analyzed. A 2nd-order equivalent model is introduced to simplify the parameters design. By analyzing the control performance indices, the VIDC parameters are optimized. At last, based on the principle of equivalent machine, an inertia matching method of the multi-parallel bi-DC converters is proposed. The simulation results verify that ESS, by acting as a synthetic inertia, can improve the voltage dynamic characteristics and stability in islanded DC-MG. Compared with other control methods, it has better control effect.

*Index Terms*—DC microgrid, synthetic inertia, energy storage system, DC voltage oscillation, parameter design.

## I. INTRODUCTION

E NERGY scarcity and related environmental issues are becoming serious problems around the world. Developing

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renewable and clean energy provides a good solution to these problems. Power converters are the key to renewable energy generation (REG) integration to microgrid (MG) [1], [2], and power converters as grid interfaces are replacing conventional synchronous generators (SG) [3], [4]. However, presently, the power system inertia is solely contributed by the rotating masses of SG. As a result, the lack of inertia may challenge the operation and control of modern power systems, leading to the frequency instability in alternating current microgrid (AC-MG) [5] and/or the voltage instability in direct current microgrid (DC-MG) [12], [23].

In conventional power systems, the grid frequency reveals the degree of balancing between generation and demand, SGs autonomously slow down or speed up in accordance with the grid frequency [4]. In this way, SGs release/absorb the energy to/from the power grid so that the power mismatch can be compensated partially. This effect is quantitatively evaluated by the per unit kinetic energy, which is defined as the power system inertia [6], [7]. However, as the penetration levels of REG grow, inertia decreases. This is because REGs are normally coupled to the power grid through power electronics devices without any rotational inertia [8]. There is no kinetic energy that can be used as rotational inertia in such power conversion systems [9]. As more SGs are phased out and replaced by power converters, the entire power system becomes more inertia-less, which becomes a major concern for the system stability and converter control [10]. In DC-MG, its inertia manifests the ability to prevent sudden changes of DC voltage [11]. More specifically, due to the presence of the interface converter with fast response ability, the DC bus voltage may easily oscillate beyond the acceptable range, leading to generation tripping, undesirable load shedding, or even system collapses [12]. This means DC-MG does not have sufficient inertia to stabilize the DC bus voltage. Therefore, it is necessary to develop various measures to improve the dynamic response.

Various control strategies to tackle the issue of lacking inertia have already been proposed, including the inertia-emulation techniques. Virtual inertia control is primarily emphasised on providing an effective frequency support to AC grid. The inertial dynamics of virtual-synchronous-controlled doubly fed induction generator (DFIG)-based wind turbines (WT) is investigated in [16]. Thus DFIG-based WT can provide the desired inertial support to power grid. In [17], an oscillation damping approach is developed for distributed generators to control inverters to

0885-8969 © 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information. behave like a synchronous generator producing virtual inertia during a short operation time. A derivative control-based virtual inertia is introduced in [18], and the virtual inertia makes a considerable improvement on first overshoot responses and damping characteristics of high voltage direct current (HVDC) links.

However, none of the works mentioned above involves the solutions of inertia reduction in DC-MG. In DC-MG, connecting capacitors is a straightforward approach but will bring additional power losses, and is limited by certain application scenarios with limited space, such as: ship electrical systems [13]. In [14], a droop scheme is proposed and thus DC sources can be coordinated together with the frequency of the AC voltage, like SGs in conventional power systems. In [15], a virtual impedance loop is utilized to improve the dynamic performance of the power sharing control unit. Inevitably, conventional active methods need a strong trade-off between effective active compensation and reducing the dynamic coupling, and the stability margin may be impacted. By the AC/DC analogy, virtual inertia emulation technique has been developed in DC-MG. The virtual inertia of DC-MG can be enhanced by the kinetic energy in the rotor of the permanent magnet synchronous generators (PMSG) based wind turbine, the energy stored in energy storage system (ESS) and/or capacitors, and the energy from the utility grid [12]. Therefore, the output power of converters can be changed in response to the DC bus voltage during power fluctuations [16], [19]. In [11], a virtual inertia control strategy for bidirectional grid-connected converters is proposed to enhance the inertia of the DC-MG and the parameters design is discussed. A virtual synchronous generator control strategy is introduced to dampen DC-side oscillations in a wide frequency region and enhance the inertia of DC network [20]. In [21], a virtual capacitor control, which utilizes the energy storage capability of the modular multilevel converter to attenuate voltage fluctuations of HVDC systems, is proposed. The virtual inertia control in previous works only simulated the swing equation of the SG or the energy conversion form of capacitors to control the external characteristic of converter, which is essentially a virtual capacitor control. Therefore, new control strategies suitable for DC microgrid are needed, based on the model of DC machine.

A concept to operate bidirectional DC (bi-DC) converters of ESS as DC machine to achieve rotor inertia emulation and regulate the DC bus voltage fluctuations is proposed in [22]. However, the concept model is actually not clear, controller structure and the parameters design are complicated, and the multi-parallel operation is not analyzed. Besides, the output of the inertia loop is the output voltage reference of bi-DC converter, which impacts the static characteristic. [23] proposes a virtual inertia control (VIC) for photovoltaic arrays (PVAs) to enhance the inertia of a hybrid PVA-battery DC-MG. Virtual inertia matching method of the parallel virtual SGs is proposed in [24] to ensure the transition process remains synchronized. To sum up, virtual inertia controls are developed for DC grid, but this technique is incomplete in theoretical and practical regards, and the matching method and stable region parameters design need to be further investigated. Hence, it deserves to be explored by researchers and engineers.

TABLE I System Parameters of the Studied DC-MG

Subsystem	Parameters	Magnitude	
	Input voltage $v_s$	100 V	
Bidirectional DC converter	Input filter inductor $L_{\rm s}/R_{\rm s}$	5 mH/0.01 Ω	
	Capacitance $C_{out}$	3000 μF	
	Switching frequency	10 kHz	
Buck converter	Load voltage vout buck	100 V	
	Load power $P_{\text{const}}(R)$	2000 W(5Ω)	
	Input capacitance $C_{in}$	1200 µF	
	Filter inductor $L_{\rm f}/R_{\rm f}$	4 mH/0.01 Ω	
	Output capacitance $C_{\rm f}$	1000 μF	
DC bus	DC bus voltage $v_{dc_{bus}}$	300 V	
	DC bus capacitance $C_{\text{bus}}$	3000 μF	
	Line impedance $R_{\text{line}}/L_{\text{line}}$	0.01 Ω/0.1 mH	

TABLE II ANALOGY BETWEEN DC MACHINE AND VIDC

Physical meaning	DC Machine	Proposed VDCM
Mechanical power	Primary motor	ESS
Moment of inertia	Rotor $(J_{dc})$	$C_{\rm vir} \left( J_{\rm vir} \right)$
Damping source	The friction $(D_{damp})$	$i_{\rm vir} \left( D_{\rm d} \right)$
Armature winding	R <sub>a m</sub>	$R_{\mathrm{a}}$
Excitation winding	$R_{ m f}$	$R_{ m s}$
Angular velocity	ω	$\omega_{ m vir}$
Output voltage	V <sub>out_m</sub>	$v_{out}$
Excitation constant	$C_{\mathrm{T}} \circ \varphi_{\mathrm{m}}$	$C_{\mathrm{T}} \cdot \varphi$

This paper studies the provision of a dynamic voltage support ability by ESS and proposes a virtual inertia and damping control (VIDC) strategy. Without modifications of system hardware, inertia can be synthesized by the energy stored in ESS to mitigate voltage oscillation caused by power disturbance. Virtual inertia power and damping power are provided by the ESS without increasing system cost and complexity, since ESS are always necessary in islanded DC-MG for voltage stabilizing. It is worth noting that the proposed VIDC strategy is derived based on the physical model of the DC machine, instead of the swing characteristic of SG. The concept, implementation, stability analysis, inertia matching method of the VIDC strategy and parameter design are studied in detail. In addition, based on the principle of equivalent DC machine, it is easier to achieve inertia matching of multi-parallel bi-DC converters controlled by VIDC. The major contributions of this work are:

- 1) Based on a simple DC machine model, a VIDC strategy is proposed in this paper. It is, in nature, a systematic combination of active damping control, virtual resistance control and virtual inertia control.
- The analogy between DC machine and bi-DC converter control system is addressed in detail and the VIDC concept model is proposed. The control parameters have a clear physical meaning, as shown in Table II.
- 3) The rated voltage is added into the inertia loop, thus, the proposed VIDC strategy only acts in the transient process with a better control performance, the static characteristic (i.e., voltage regulation and power sharing) would not be affected.
- The inertia matching method of multi-parallel bi-DC converters is analyzed to realize dynamic process consistency.



Fig. 1. Topology of the studied DC-MG in islanded mode.



Fig. 2. Circuit of DC converter. (a) bi-DC converter, (b) buck converter.

 Parameters design methods are given. A second-order model is proposed to simplify the parameter design.

The rest of this paper is organized as follows. Section II presents the studied DC-MG topology. In Section III, the inertia source of DC-MG is analysed and the VIDC strategy for bi-DC converter is proposed. The small signal model of bi-DC converters control system is established and the dynamic performance of VIDC is analysed in Section IV. Section V discusses details on parameter design. In Section VI, simulation results verify the theoretical analysis. Finally, some conclusions are given in Section VII.

#### II. TOPOLOGY OF THE STUDIED DC-MG AND SIMPLIFICATION

A typical DC-MG system studied in this paper is shown in Fig. 1. It composes of a group of REG, an ESS (i.e., battery in this paper) and multiple constant power loads (CPLs). The structure of the bi-DC converter that applied in both the REG and the ESS is shown in Fig. 2(a). The dual loop control strategy is applied for the ESS control, while the constant power control strategy (where only the current inner loop is reserved) is applied for the REG. The structure of the buck converter for the CPLs is shown in Fig. 2(b). The buck converter attaching to a resistor R also adopts a dual loop control strategy. It regulates its output voltage to simulate a CPL. The corresponding parameters of the above convertors are shown in Table I. The DC voltage source



Fig. 3. The simplified model of bi-DC converter (a) switching cycle average model (b) simplified circuit of bi-DC converter.



Fig. 4. Inertia mapping between the DC machine and capacitor. (a) DC machine model, (b) DC capacitor.

 $v_{\rm s}$  serves as the power source of ESS.  $i_{\rm m}$  is the output current of the source.  $i_{\rm out}$  and  $v_{\rm out}$  are the output current and output voltage of the bi-DC converter.

$$\begin{cases} L_{\rm s} \frac{\mathrm{d}\Delta i_{\rm m}}{\mathrm{d}t} = \Delta v_{\rm s} - d^* \Delta v_{\rm out} + V_{\rm out} \Delta d^* - R_{\rm s} \Delta i_{\rm m} \\ C_{\rm out} \frac{\mathrm{d}\Delta v_{\rm out}}{\mathrm{d}t} = d^* \Delta i_{\rm m} - I_{\rm out} \Delta d^* - \Delta i_{\rm out} \end{cases}$$
(1)

$$\begin{cases} L_{\rm s} \frac{\mathrm{d}I_{\rm m}}{\mathrm{d}t} = V_{\rm s} - d^* V_{\rm out} - R_{\rm s} I_{\rm m} \\ C_{\rm out} \frac{\mathrm{d}V_{\rm out}}{\mathrm{d}t} = d^* I_{\rm m} - I_{\rm out} \end{cases}$$
(2)

The state equation of the bi-DC converter and the steady-state operating point equation are shown in (1) and (2). When the loss of the switching network is neglected, the switching network in the bi-DC converter can be replaced by an ideal transformer. In this case, the switching cycle average model of bi-DC converter can be obtained in Fig. 3(a). Based on (2), the ratio of the ideal transformer is  $d^*$ :1. The superscript '' represent the physical quantity of the primary side derived to the secondary side. At this time, the simplified circuit can be obtained and shown in Fig. 3(b) where  $\Delta v'_{\rm s} = (\Delta v_{\rm s} + V_{\rm out} \Delta d^*)/d^*$ ,  $Z'_{\rm s} = Z_{\rm s}/d^{*2}$  and  $\Delta t'_{\rm m} = \Delta t_{\rm m} d^*$ . And d is the duty and  $d^* = 1 - d$ .

# III. INERTIA SOURCE IN DC-MG AND VIDC STRATEGY

## A. Inertia Source Analysis in DC-MG

1) DC Machine: The DC machine model is shown in Fig. 4(a).  $v_{\rm f}$ ,  $i_{\rm f}$  and  $R_{\rm f}$  are excitation voltage, excitation current, and field winding resistance, respectively. The equivalent circuit equation, torque balance equation and power balance equation are in (3) and (4). E,  $R_{\rm a_m}$ ,  $i_{\rm out_m}$  and  $v_{\rm out_m}$  are the internal potential, the winding resistance, the output current and the output voltage of the armature winding.  $D_{\rm damp}$  and  $J_{\rm dc}$  are damping coefficient and inertia coefficient.  $\omega$  is the rotor speed and  $\omega_{\rm on_m}$  is its rated value.  $C_{\rm T_m}$  and  $\varphi_{\rm m}$  are torque coefficient and magnetic flux.  $P_{\rm m}$  and  $P_{\rm e_m}$  are mechanical power and electromagnetic power, respectively; and  $T_{\rm m}$  and  $T_{\rm e_m}$  are mechanical torque and electromagnetic torque, respectively.  $v_{\rm on}$  is the rated output voltage. It can be found in (4b) that when the DC machine is disturbed, rotor compensates the power difference by absorbing or releasing kinetic energy, suppressing the fluctuation of  $v_{out}$ .

$$\begin{cases} v_{\text{out}\_m} = E - R_{a\_m} i_{\text{out}\_m} \\ E = C_{T\_m} T_{e} = C_{T\_m} \varphi_m \omega \end{cases}$$
(3)

$$T_{\rm m} - T_{\rm e_m} - D_{\rm damp} \left( \omega - \omega_{\rm on_m} \right) = J_{\rm dc} \frac{\mathrm{d}\omega}{\mathrm{d}t}$$
(4a)

$$\begin{cases} P_{\rm m} - P_{\rm e_m} - \frac{\omega_{\rm on_m} D_{\rm damp}}{C_T \varphi} \left( E - v_{\rm on} \right) = \frac{\omega_{\rm on_m} J_{\rm dc}}{C_T \varphi} \frac{\mathrm{d}(E - v_{\rm on})}{\mathrm{d}t} \\ P_{\rm d} = \frac{\omega_{\rm on_m} D_{\rm damp}}{C_T \varphi} \left( E - v_{\rm on} \right) \\ P_{\rm iner_m} = \frac{\omega_{\rm on_m} J_{\rm dc}}{C_T \varphi} \frac{\mathrm{d}(E - v_{\rm on})}{\mathrm{d}t} \end{cases}$$

$$(4b)$$

$$P_{\rm e_m} = \omega T_{\rm e_m} \approx \omega_{\rm on_m} T_{\rm e_m} \tag{4c}$$

2) *DC Capacitor:* The power balance at the DC capacitor is shown in Fig. 4(b) and can be expressed in (5).

$$P_{\rm in} - P_{\rm out} = C_{\rm out} \, V_{\rm dcn} \frac{\mathrm{d}v_{\rm out}}{\mathrm{d}t} \approx C_{\rm out} V_{\rm dcn} \frac{\mathrm{d}v_{\rm out}}{\mathrm{d}t} \qquad (5)$$

where  $P_{\rm in}$  is the power output from the converter;  $P_{\rm out}$  is the power injected into the DC-MG;  $v_{\rm out}$  is the DC output voltage;  $V_{\rm dcn}$  is the rated value of DC output voltage;  $C_{\rm out}$  is the DC capacitor. When the DC-MG operates in a steady state, the DC voltage maintains constant,  $P_{\rm in} = P_{\rm out}$ . Suppose that  $P_{\rm out}$  changes by  $\Delta P_{\rm out}$ , the unbalanced power will cause  $C_{\rm out}$  to discharge or charge. When  $C_{\rm out}$  is large enough, the change rate and deviation of  $v_{\rm out}$  can be reduced. Limited by the actual capacity of  $C_{\rm out}$ , the inertia of DC-MG is small, and the DC voltage might fluctuate drastically.

The inertia mapping between DC machine and DC capacitors is shown in Fig. 4. The inertia constant of the DC machine  $H_r$  is defined as the ratio of the kinetic energy in the rotating masses ( $J_{dc}\omega^2$  on/2) to its rated power  $S_{base}$ . Similarly, the inertia constant of the capacitor  $H_c$  can be defined as the ratio of the electrical energy stored in the capacitor ( $C_{out} v^2 out/2$ ) to its rated power  $S_{base}$ .

# B. VIDC Concept Model and Its Implementation

Considering the potential inertia supply ability of ESS [16], a VIDC strategy for bi-DC converter is proposed based on the voltage inertia characteristics of the DC machine and capacitors. The physical nature of this control is to properly regulate ESS to release or absorb energy in the same way as the rotors of DC machine and capacitors do, and connect a virtual resistance in series with the output port, then alleviate the DC bus voltage oscillation. By comparing (4) and (5), the control equation is shown in (6).

$$\begin{cases} P_{\rm vm} - P_{\rm e} - \frac{D_{\rm d}\omega_{\rm on}}{C_T\varphi} \left( v_{\rm vir} - V_{\rm dcn} \right) \approx \frac{\omega_{\rm on}J_{\rm vir}}{C_T\varphi} \frac{d(v_{\rm vir} - V_{\rm dcn})}{dt} \\ P_{\rm vd} = \frac{D_{\rm d}\omega_{\rm on}}{C_T\varphi} \left( v_{\rm vir} - V_{\rm dcn} \right) \\ P_{\rm iner} = \frac{\omega_{\rm on}J_{\rm vir}}{C_T\varphi} \frac{d(v_{\rm vir} - V_{\rm dcn})}{dt} = C_{\rm vir} V_{\rm dcn} \frac{d(v_{\rm vir} - V_{\rm dcn})}{dt} \end{cases}$$
(6a)

$$P_{\rm e} = \omega_{\rm vir} T_{\rm e} = i_{\rm out} v_{\rm out} \tag{6b}$$

$$\begin{cases} v_{\text{out}} = v_{\text{vir}} - R_{\text{a}}i_{\text{out}} \\ v_{\text{vir}} = C_{\text{T}} \varphi \omega_{\text{vir}} \end{cases}$$
(6c)



Fig. 5. Concept model and block diagram of VIDC strategy. (a) concept model. (b) control block diagram. (c) virtual inertia and damping emulation part.

where  $V_{\rm dcn}$  is the rated output voltage of bi-DC converter.  $P_{\rm vm}$ is the input power of converter, which includes  $P_{\rm vd}$  (the virtual damping power),  $P_{\rm e}$  (the output electromagnetic power) and  $P_{\text{iner}}$  (the virtual inertia power).  $J_{\text{vir}}$  is the introduced inertia coefficient of VIDC and  $C_{vir}$  is the equivalent virtual capacitor.  $D_{\rm d}$  is the virtual damping coefficient.  $v_{\rm vir}$  is the virtual internal potential in the VIDC strategy, emulating E of DC machine.  $R_{\rm a}$  is a virtual resistance. The physical significance of (6) is to transform the relationship between the torque balance and  $\omega_{\rm vir}$  into the relationship between the power balance and  $v_{\rm vir}$ , and it also reflects the inertia and damping characteristics of the bi-DC converter. When there exists power mismatch, the virtual (static) rotor  $C_{\rm vir}$  can suppress the voltage oscillation by absorbing or releasing power. The damping power  $P_{\rm vd}$  is provided until the power balance is achieved again. The VIDC concept model could be derived in Fig. 5(a).

Based on the VIDC concept model in Fig. 5(a), the analogy between DC machine and the bi-DC converter control system is shown in Table II. The energy of the DC machine is provided by the prime mover, while the inertia power and the damping power of the bi-DC converter come from ESS, and the input filter imitate the excitation winding. The introduction of virtual inertia  $J_{vir}$  is equivalent to connecting a virtual capacitor  $C_{vir}$ in parallel on the converter output side, which is regarded as the virtual (static) rotor of the bi-DC converter, providing inertia of smoothing voltage fluctuation.  $R_a$  is an adjustable parameter that mimics armature winding resistance (the loss of the switching network).  $D_{\rm d}$  is equivalent to a controlled current source  $i_{\rm vir}$ , simulating the friction effect. When the voltage rises, the virtual damping current source  $i_{\rm vir}$  absorbs the surplus power and vice versa. Besides, bi-DC converters controlled by VIDC can operate in generator or motor mode, as DC machine can do.

The diagram of the VIDC strategy for bi-DC converter is shown in Fig. 5(b), including restoring part (voltage outer loop,  $G_v(s) = k_{vp} + k_{vi}/s$ ), current inner loop ( $G_i(s) = k_{ip} + k_{ii}/s$ ), and inertia and damping emulation part which includes mechanical part (Eq. 6(a-b)) and electrical part (Eq. 6(c)).

*Voltage restoring part:* The objective of restoration controller is to restore  $v_{out}$  to its reference value  $v_{ref}$ . In the restoring part, a PI controller  $G_v(s)$  is adopted to generate deviation power  $\Delta P_e$ using the error defined between  $v_{out}$  and  $v_{ref}$ . Due to  $G_v(s)$ ,  $v_{out}$  would always track its reference value  $v_{ref}$ , which means the steady-state error can be eliminated, achieving the voltage restoration. The summation of  $\Delta P_e$  and the feedback power  $P_e$ form  $P_{vm}$ , i.e., the input signal for VIDC part.

*VIDC loop:* As shown in Fig. 5(c), the VIDC loop consists of two parts: the virtual inertia control loop (mechanical part) and the armature winding emulation part (electrical part). (1) In the mechanical part, the virtual speed  $\omega_{vir}$  of the (static) rotor  $C_{vir}$  is controlled according to the power balance equation, achieving the inertia and damping emulation. And its output is the virtual speed  $\omega_{vir}$ , i.e., the input signal for the electrical part. (2) In the electrical part, the virtual internal potential  $v_{vir}$  is derived and then the output current reference value  $i_{o'ref}$  is obtained according to the armature winding circuit equation.  $k = V_{dcn}/V_s$  is introduced to achieve the conversion between output current and input current  $i_{m'ref}$  (namely, the reference value of the current inner loop).

*Current inner loop*: The objective of current inner loop is to restore  $i_{\rm m}$  to its reference value  $i_{\rm m'ref}$ . In this part, a PI controller  $G_{\rm i}(s)$  is adopted to generate the duty ratio, using the error defined between  $i_{\rm m}$  and  $i_{\rm m'ref}$ . Due to the existence of  $G_{\rm i}(s)$ , the actual value of  $i_{\rm m}$  would always track its reference value  $i_{\rm m'ref}$ , which means the steady-state error of current can be eliminated and the output voltage can be controlled indirectly.

The control system dynamic response is affected by  $J_{\rm vir}$  and  $D_{\rm d}$  which provide extra freedom degrees. The VIDC loop is equivalent to connect an adjustable capacitor and controlled current source in parallel at the output side of the converter, and  $R_{\rm a}$  is a virtual resistance in series with the output port.

Assuming that  $P_{vm}$  changes by  $\Delta P_{vm}$ , the unbalanced power will be compensated by three parts:

$$\Delta P_{\rm vm} = \Delta P_{\rm vd} + \Delta P_{\rm iner} + C_{\rm out} V_{\rm dcn} \frac{\mathrm{d}v_{\rm out}}{\mathrm{d}t} \tag{7}$$

As can be seen from (7),  $\Delta P_{\rm vm}$  can be balanced by  $\Delta P_{\rm vd}$ ,  $\Delta P_{\rm iner}$  and the power from capacitor  $C_{\rm out}$ . Since  $\Delta P_{\rm vd}$  and  $\Delta P_{\rm iner}$ , which is from ESS, are able to take on most unbalanced power, the power from  $C_{\rm out}$  will be reduced, i.e., for the same  $\Delta P_{\rm vm}$ , the change rate and deviation of the  $v_{\rm out}$  can be reduced and the inertia and damping of DC-MG are improved.



Fig. 6. Droop control and circulating current analysis. (a) concept model. (b) control block diagram (c) equivalent circuit.

## C. Droop Control for Multi-Parallel Operation

To achieve multi-parallel operation of bi-DC converters, droop control is added in outer loop, as shown in in Fig. 6(a) and Fig. 6(b).  $v_{\text{max}}$ ,  $v_{\text{min}}$ ,  $i_{\text{m}_{\text{max}}}$ , and  $i_{\text{m}_{\text{min}}}$  are the maximum and minimum values of  $v_{\text{out}}$ , the maximum discharge current and the maximum charge current of ESS, respectively. And  $R_{\text{d}}$  is the droop coefficient. The V-I droop control equation is shown in (8). Current sharing between bi-DC converters is inversely proportional to  $R_{\text{d}}$ . As shown in Fig. 6(c), due to the imbalance in the voltage drop across the line resistance, a circulating current would form between the bi-DC converters, which affects the even power sharing. Circulating current  $\Delta i_{\text{cir}}$ can be calculated by (9). This article focuses on the problem of voltage fluctuations, and the suppression method of circulating current is not discussed in detail.

$$v_{\rm out} = v_{\rm ref} = V_{\rm dcn} - R_{\rm d} i_{\rm m} \tag{8}$$

$$\Delta i_{\rm cir} = \frac{R_{\rm line2} - R_{\rm line1} R_{\rm d2} / R_{\rm d1}}{R_{\rm line1} + R_{\rm line2}} i_{\rm out2} \tag{9}$$

# IV. SMALL SIGNAL MODEL AND DYNAMIC CHARACTERISTIC ANALYSIS OF THE VIDC STRATEGY

To study the relationship between  $v_{out}$  and power demand, the small signal model of the bi-DC converter is established. Neglecting the energy loss, there is:

$$v_{\rm m} \, i_{\rm m} = v_{\rm out} \left( i_{\rm out} + C_{\rm out} \frac{\mathrm{d} v_{\rm out}}{\mathrm{d} t} \right)$$
(10)

The relation between  $\Delta i_{\rm m}$  and  $\Delta i_{\rm out}$  is expressed as:

$$\frac{\Delta i_{\text{out}}\left(s\right)}{\Delta i_{\text{m}}\left(s\right)} = \frac{V_{\text{s}}}{V_{\text{dcn}}} = A_{\text{i}}\left(s\right) \tag{11}$$

From (6b), the small signal model of  $\Delta T_{\rm e}$  is obtained:

$$\Delta T_{\rm e} = \frac{I_{\rm out}}{\omega_{\rm on}} \Delta v_{\rm out} + \frac{V_{\rm out}}{\omega_{\rm on}} \Delta i_{\rm out} - \frac{V_{\rm out}I_{\rm out}}{\omega_{\rm on}^2} \Delta \omega \qquad (12)$$

Based on (10), (11), (12) and Fig. 5, the small signal model of the bi-DC converter control system can be obtained, as shown in Fig. 7.  $K_{pwm}$  is the equivalent gain of pulse width modulator (PWM).  $\Delta i_{out}$  affects  $\Delta v_{out}$  through three loops. The transfer function of  $\Delta v_{out}$  and  $\Delta i_{out}$  can be split into three parts:

$$TF(s) = \frac{\Delta v_{\text{out}}}{\Delta i_{\text{out}}} = TF_{\text{lp1}}(s) + TF_{\text{lp2}}(s) + TF_{\text{lp3}}(s)$$
(13)



Fig. 7. Small signal model of the bi-DC converter control system.

The transfer functions of these three loops are derived as:

$$TF_{\rm lp1}(s) = \frac{V_{\rm dcn}k \cdot C_{\rm T}\varphi \cdot T_{\rm iv}(s) \cdot T_{\rm vi}(s)}{\omega_{\rm on}\left(R_{\rm a} + k \cdot H_{\rm vir} - k \cdot C_{\rm T}\varphi \cdot T_{\rm iv}(s)T_{\rm vi}(s)\right)}$$
$$= -TF_{\rm lp2}(s)$$
(14a)

$$TF_{\rm lp3}\left(s\right) = \frac{\Delta v_{\rm out}}{\Delta i_{\rm out3}} = -\frac{T_{\rm vi}\left(s\right)A_{\rm i}\left(s\right)}{1 - T_{\rm iv}\left(s\right) \cdot T_{\rm vi}\left(s\right)}$$
(14b)

where  $T_{vi}(s)$ ,  $T_{iv}(s)$   $G_{vd}(s)$ ,  $G_{isd}(s)$  and  $H_{vir}(s)$  are in (15) and (16). The influences of  $\Delta i_{out1}$  and  $\Delta i_{out2}$  on the  $\Delta v_{out}$ can cancel each other out as shown in (14a). Thus,  $TF(s) = TF_{1p3}(s)$ . The physical significance of TF(s) is to reflect how  $v_{out}$  will change when the output current  $i_{out}$  suddenly increases or decreases. As is known to all,  $i_{out}$  is relevant to the power demand of the DC-MG and decided by the power consumption of the loads and the output power of DGs and ESS.

$$G_{\rm vd}(s) = \frac{\Delta v_{\rm out}}{\Delta d} |_{\Delta v_{\rm s}=0,\Delta i_{\rm out}=0}$$
$$= \frac{-i_{\rm m} \left(R_{\rm s} + sL_{\rm s}\right) + \left(1 - d\right) v_{\rm out}}{s^2 L_{\rm s} C_{\rm out} + sR_{\rm s} C_{\rm out} + \left(1 - d\right)^2}$$
(15a)

$$G_{\text{isd}}(s) = \frac{\Delta i_{\text{m}}}{\Delta d} |_{\Delta v_{\text{s}}=0,\Delta i_{\text{out}}=0}$$
$$= \frac{sC_{\text{out}}v_{\text{out}} + (1-d)i_{\text{m}}}{s^{2}L_{\text{s}}C_{\text{out}} + sR_{\text{s}}C_{\text{out}} + (1-d)^{2}}$$
(15b)

$$\begin{cases} T_{\rm vi}\left(s\right) = -\left(T_{\rm vT}\left(s\right) \cdot T_{\rm v\omega}\left(s\right) - 1\right)\frac{k}{R_a}\\ T_{\rm vT}\left(s\right) = -\frac{2I_{\rm out} + V_{\rm den}G_{\rm v}(s)}{\omega_{\rm on}^2 H_{\rm vir}(s)}\\ T_{\rm v\omega}\left(s\right) = \frac{\omega_{\rm on}^2 H_{\rm vir}(s)}{\omega_{\rm on}^2 + H_{\rm vir}(s)I_{\rm out}V_{\rm den}} \end{cases}$$
(15c)

$$T_{\rm iv}\left(s\right) = \frac{G_{\rm i}\left(s\right)G_{\rm vd}\left(s\right)}{V_{\rm den} + G_{\rm i}\left(s\right)G_{\rm isd}\left(s\right)} \tag{15d}$$

$$H_{\rm vir}\left(s\right) = \frac{1}{s/J_{\rm vir} + D_{\rm d}} \tag{16}$$

Fig. 8 shows the zeros and dominant poles distribution of TF(s). The symbol "×" represent poles. The symbol "o" represents zero. It can be observed that the pair of poles in the red circle are far away from the point (0, 0) in Fig. 8 and almost stay constant when  $J_{vir}$  or  $D_d$  changes. Besides, there is a pair of zeros near this pair of poles, which constitutes dipoles with this pair of poles and neutralizes the influence of this pair of poles. Hence, their influence can be neglected. In Fig. 8(a), the oscillation frequency firstly increases and then decreases with  $J_{vir}$  increasing. When  $J_{vir} = 6$ , the system becomes overdamped. After that, the dominant poles become two negative real roots.



Fig. 8. Zero and dominant poles distribution of TF(s). (a) arrow direction: Jvir changing from 0.05 to 10. (b) arrow direction: Dd changing from 0.05 to 10.

One pole gradually moves away from the imaginary axis, and the other one moves toward the imaginary axis but will not cross the imaginary axis, becoming the only dominant pole. The time constant and the system inertia increase with  $J_{vir}$  increasing. The same trend with  $D_d$  increasing can be observed in Fig. 8(b). There is only one pair of dominant poles, which means the high-order system can be estimated by the performance indices of a 2nd-order system.

#### V. PARAMETERS DESIGN

### A. Design of Voltage Outer Loop and Current Inner Loop

With a large control bandwidth, the current loop provides fast tracking performance of  $i_{out}$ . The voltage loop ensures accurate reference tracking, with a much slower dynamic response than the current loop. Small signal models of current loop and voltage loop are in Fig. 9(a) and Fig. 9(b), respectively. The cut-off frequency of the current loop  $f_{cc}$  should be no greater than one-tenth of the switching frequency  $f_{s}$ . Considering  $K_{PWM} = 1$ , there is:

$$|G_{i}(s) K_{pwm}G_{isd}(s)| = 1$$
(17)



Fig. 9. Small signal model and Bode diagram. (a) Small signal model of current loop. (b) Small signal model of voltage loop. (c) Bode diagram of current loop. (d) Bode diagram of voltage loop.

The bode diagram of current loop is shown in Fig. 9(c).  $k_{ip}$  is chosen as 5 with  $f_{cc} = 636.9$ Hz and phase margin (PM) = 91.1°.

As for the voltage loop, the cut-off frequency  $f_{cv}$  should be no greater than one-tenth of  $f_{cc}$  to mitigate coupling between voltage loop and current loop. The PM is designed to be no smaller than  $\pi/4$ . Since the bandwidth of the voltage loop is much lower than the current loop, the current loop could be simplified to  $K_c = 1$  while designing voltage loop.  $H_c(s)$  is the sampling loop and equivalent to 1. Then there is:

$$|H_{\rm c}(s) G_{\rm v}(s) K_{\rm c} H_{\rm out}(s)|_{s=j2\pi f_{\rm cv}} = 1$$
 (18a)

$$\angle H_{\rm c}\left(s\right)G_{\rm v}\left(s\right)K_{\rm c}H_{\rm out}\left(s\right)|_{s=j2\pi f_{\rm cv}} \ge -\frac{3}{4} \tag{18b}$$

$$H_{\text{out}}(s) = \frac{\Delta v_{\text{out}}}{-\Delta i_{\text{out}}} |_{\Delta v_s = 0, \Delta d = 0}$$
$$= \frac{R_{\text{s}} + sL_{\text{s}}}{s^2 L_{\text{s}} C_{\text{out}} + sR_{\text{s}} C_{\text{out}} + (1 - d)^2}$$
(18c)

 $H_{\text{out}}(s)$  is the open loop output impedance of bi-DC converter. The bode diagram of the voltage loop is shown in Fig. 9(d).  $k_{\text{vp}}$ 



Fig. 10. Simplified 2nd-order model of the bi-DC converter control system.

and  $k_{vi}$  are chosen as  $k_{vp} = 0.3$ ,  $k_{vi} = 50$  with  $f_{cv} = 52.7$ Hz and phase margin (PM) = 66.4°.

#### B. Parameters Design of VIDC

The rated output voltage  $V_{\rm dcn}$  is 300 V, the rated current  $I_{\rm on}$  is 20 A, and the virtual internal potential  $v_{\rm vir} = 325$  V. The virtual resistance  $R_{\rm a} = (v_{\rm vir} - V_{\rm dcn})/I_{\rm on} = 1.25 \,\Omega.\,\omega_{\rm on}$  is chosen as 314 rad/s, then  $C_{\rm T}.\varphi$  is chosen as 0.955.  $J_{\rm vir}$  and  $D_{\rm d}$  are selected according to the requirements of the dynamic characteristic.

When the VIDC regulator is designed, the unity gain block represents the closed-loop gain of current loop with the large bandwidth. The voltage loop with a small bandwidth has slow dynamic response and cannot be ignored. To simplify the parameter design process, a simplified model of the proposed VIDC strategy is proposed in Fig. 10. The detailed transfer functions  $T_d(s)$  can be obtained in (19) shown at the bottom of this page, which is a 2nd-order system.  $k_1 = I_{out}V_{dcn}/\omega_{on}, k_2 = V_{dcn}/(\omega_{on}R_{load})$  and  $k_3 = V_{dcn}/\omega_{on}, g = R_{load}/(R_{load}-R_a)$  and  $K = C_T.\varphi$ . Its physical meaning is to reflect dynamic characteristic of  $v_{out}$  when  $i_{out}$  changes suddenly. Thus, several important performance indices in 2nd-order system for can be used to evaluate dynamic.

Based on (19), damping ratio  $\xi$  and the natural oscillation frequency  $\omega_n$  of the system can be derived as (20).

$$\omega_{\rm n} = \sqrt{\frac{J_{\rm vir}gKV_{\rm dcn}k_{\rm vi}}{\omega_{\rm on}}}$$

$$\xi = \frac{J_{\rm vir}\left(D_{\rm d} + k_1\right)\omega_{\rm on} + gK\left(k_2\omega_{\rm on} + 2I_{\rm out} + V_{\rm dcn}k_{\rm vp}\right)}{\omega_{\rm on}}$$
(20a)
$$(20b)$$

The voltage response may also be evaluated by the overshoot  $\sigma$ , which can be derived as shown in (21).

$$\sigma = \exp\left(-\frac{\pi\xi}{\sqrt{1-\xi^2}}\right) \tag{21}$$

Additionally, the settling time  $t_s$  (time for entering the 2% quasi-steady-state error band) is normally used to evaluate the

$$T_{\mathbf{d}} = \frac{\Delta v_{\mathbf{out}}}{\Delta i_{\mathbf{out}}} = \frac{k_3 \cdot g \cdot K \cdot \omega_{\mathbf{on}} \cdot s}{\omega_{\mathbf{on}}/J_{\mathbf{vir}} \cdot s^2 + \left[ (D_{\mathbf{d}} + k_1) \,\omega_{\mathbf{on}} + g \cdot K \,(k_2 \omega_{\mathbf{on}} + 2I_{\mathbf{out}} + V_{\mathbf{dcn}} k_{\mathbf{vp}}) \right] s + g \cdot K \cdot k_{\mathbf{vp}} \cdot V_{\mathbf{dcn}}} \tag{19}$$



Fig. 11. Variation range of different performance indices. (a) damping ratio  $\xi$ . (b) natural oscillation frequency. (c) overshoot. (d) setting time.

dynamics of voltage regulation, which can be derived as (22).

$$t_{\rm s} = \begin{cases} \frac{4}{\xi\omega_{\rm n}}\xi < 1\\ -\frac{3}{\operatorname{real}(\lambda_2)}\xi > 1 \end{cases}$$
(22)

Based on (20)-(22), the relationships between various performance indices and control parameters ( $J_{\rm vir}$  and  $D_{\rm d}$ ) are demonstrated in Fig. 11. In Fig. 11(a), the increasing of  $D_{\rm d}$ leads to damping ratio increasing. When in overdamped state, the system can be equivalent to the 1st-order system, meanwhile the system inertia increases gradually with the  $J_{\rm vir}$  increasing, In Fig. 11(b),  $\omega_n$  is mainly related to the parameter  $J_{vir}$ , and gradually increases with  $J_{\rm vir}$  increasing. This can be used to guide the designer in how to avoid voltage resonance. In Fig. 11(c), voltage overshoot  $\sigma$  can well be attenuated by a large value of  $D_{\rm d}$  or  $J_{\rm vir}$ . Although being effective in attenuating the voltage overshoot and oscillation, high system inertia will inevitably slow down the dynamics of voltage regulation and extend the voltage restoration process when in overdamped state, as evidenced by Fig. 11(d). Theoretically,  $D_{d}$  and  $J_{vir}$  should be designed according to the comprehensive requirements of the performance indices in (20)–(22).

The detailed design of the  $J_{\rm vir}$  and  $D_{\rm d}$  is illustrated by examples as shown in Fig. 12.

*Case I:* When a certain dynamic index is needed to meet some requirements preferentially, the corresponding values of  $J_{\rm vir}$  and  $D_{\rm d}$  can be directly obtained according to Fig. 12(a-c). (a) When the damping ratio  $\xi$  is required to be over 0.7343. The corresponding parameter set is the green region in Fig. 12(a). (b) When the setting time  $t_{\rm s}$  is required to be less than 0.1 s. The corresponding parameter set is the green region in Fig. 12(b). (c) When the overshoot  $\sigma$  is required to be less than 10%. The corresponding parameter set is the green region in Fig. 12(c). For the above situations, parameters satisfying these conditions can be obtained from corresponding sets, respectively.



Fig. 12. Parameters design when performance indices with different requirements. (a) damping ratio  $\xi$ . (b) setting time  $t_s$ . (c) overshoot  $\sigma$ . (d) intersection of solutions with different requirements.

TABLE III Control Parameters of VIDC Strategy

Parameters	Values	Parameters	Values
$v_{\rm max}$	310 V	$v_{ m min}$	290 V
i <sub>m max</sub>	40 A	$i_{ m m~min}$	-40 A
$\overline{V}_{den}$	300 V	$\overline{k}_{vp}$	0.3
$C_{\mathrm{T}} \cdot \varphi$	0.955	$k_{ m vi}$	50
$J_{ m vir}$	10	$k_{ m ip}$	5.0
$D_{ m d}$	3	$R_{ m d}$	0.5
Switch frequency	10 kHz	Sampling frequency	10 kHz

*Case II:* When the three performance indices are required to meet some certain requirements at the same time, the parameters can be obtained from the intersection of their respective solutions. For example, when  $\xi > 0.7343$ ,  $t_s > 0.1$  s and  $\sigma < 10\%$  are required at the same time, the solution is the intersection of the green regions in Fig. 12(a-c), i.e., the shadow region in Fig. 12(d).

According to (20b), when  $\xi$  is required to be 0.7343,  $J_{\rm vir}$  could be 10 and  $D_{\rm d}$  could be 3 as shown in Fig. 12(a). The control parameters are shown in Table III.

## C. Inertia Matching Method

This section will focus on matching the inertia parameter to make the voltage transition process of multi-parallel bi-DC converters consistent and improve their transient stability. Then equation (6) will be simplified to:

$$P_{\rm vm} - P_{\rm e} \approx \frac{\omega_{\rm on} J_{\rm vir}}{C_{\rm T} \varphi} \frac{\mathrm{d} v_{\rm out}}{\mathrm{d} t}$$
 (23)

It is assumed that the bi-DC converter operates at the steadystate operating point  $S_1$  before the disturbance occurs, as shown



Fig. 13. Block diagram of  $V^2$ -*P*-based virtual inertia control.

 TABLE IV

 CONTROL PARAMETERS OF DUAL CONTROL AND  $V^2$ -P-Based VIC

Control strategy	Parameters		Magnitude
	Droop coefficient $k_i$		0.01
	voltage	Proportional gain $k_{vp}$	0.2
Dual loop control	loop	Integral gain $k_{vi}$	0.02
	current	Proportional gain $k_{ip}$	5
	loop	Integral gain $k_{ii}$	5
V <sup>2</sup> -P-based virtual	Droop coefficient $k_i$		2
	Sampling period $T_s$		10e-4 s
	Virtual capacitance $C_{\rm vir}$		2 F
mertia control	control current loop	Proportional gain $k_{ip}$	0.1
		Integral gain $k_{ii}$	10

in equation (24). After the disturbance occurs, it operates at the steady-state operating point  $S_2$  as shown in equation (25). When the system reaches steady state,  $P_{m1} = P_{e1}$  and  $P_{m2} = P_{e2}$ .

$$P_{\rm m1} - P_{\rm e1} \approx \frac{\omega_{\rm on} J_{\rm vir}}{C_{\rm T} \varphi} \frac{\mathrm{d} v_{\rm out}}{\mathrm{d} t} S_1 \tag{24}$$

$$P_{\rm m2} - P_{\rm e2} \approx \frac{\omega_{\rm on} J_{\rm vir}}{C_{\rm T} \varphi} \frac{\mathrm{d} v_{\rm out}}{\mathrm{d} t} S_2$$
 (25)

According to the droop control principle, when disturbances occur, output power changes from  $P_{e1}$  to  $P_{e2}$ , and the operating point moves from  $S_1$  to  $S_2$ . Inertia configuration principle is obtained, as shown in (26). When the disturbance causes voltage fluctuation in DC-MG with multi-parallel bi-DC converters, each inertia parameter must be configured in inverse proportion to the droop factor to obtain the same transition time  $\Delta t$  during the same voltage fluctuation.

$$\frac{\omega_{\rm on} J_{\rm vir}}{C_{\rm T} \varphi} \frac{\mathrm{d} v_{\rm out}}{\mathrm{d} t} \approx \frac{\omega_{\rm on} J_{\rm vir}}{C_{\rm T} \varphi} \frac{\Delta v_{\rm out}}{\Delta t} = P_{\rm m1} - P_{\rm e1} = -\Delta P$$
(26)

## VI. SIMULATION VERIFICATION

To test the proposed VIDC strategy, an islanded DC-MG system is modelled in MATLAB, as shown in Fig. 1. The parameters are in Table III.

## A. Comparison Between Different Control Methods

The VIDC strategy is compared with  $V^2$ -*P*-based VIC [12] shown in Fig. 13 and dual loop control shown in Fig. 2. Control parameters for dual loop control and  $V^2$ -*P*-based VIC can be obtained from Table IV. When t = 1.5 s,  $P_{\text{const}}$  increases 500 W suddenly and when t = 3 s,  $P_{\text{const}}$  decreases 500 W. The simulation results are shown in Fig. 14. When power disturbance occurs, the  $v_{\text{out}}$  is prone to oscillation with the droop control. In contrast, the DC voltage oscillation is effectively suppressed, when  $V^2$ -*P*-based virtual inertia control or VIDC strategy is



Fig. 14. Comparison of different control strategies.



Fig. 15. The simulation results during sudden power change. (a) REG. (b) CPL.

utilized and DC voltage is stabilized within the shortest time when VIDC strategy works. In addition, compared with the  $V^2$ -*P*-based VIC in [12], VIDC strategy has two degrees of freedom ( $J_{vir}$  and  $D_d$ ) to adjust dynamic processes, while  $V^2$ -*P*-based the virtual inertia control only has one control variable  $C_{vir}$  affecting the dynamic process.

#### B. Stand-Alone Operation Mode of bi-DC Converter

Fig. 15 are the simulation results of DC voltage oscillation caused by power disturbance on REG side and CPL side, respectively. In Fig. 15(a), When t = 1.5 s, the output power of REG  $P_{\rm pv}$  decreases 300 W suddenly and when t = 3 s  $P_{\rm pv}$  increases 300 W. In Fig. 15(b), When t = 1.5 s, the power demand of CPL  $P_{\rm const}$  increases 500 W suddenly, and when t = 3 s,  $P_{\rm const}$  decreases 500 W. When  $D_{\rm d}$  and  $J_{\rm vir}$  are set as a small value,  $v_{\rm out}$  will stabilize after a period of oscillation, indicating system inertia enhancement and damping improvement by the VIDC strategy is not obvious. The oscillation is well dampened with a good dynamic response when  $D_{\rm d}$  or  $J_{\rm vir}$  is increased.

The converter system is a strongly nonlinear system. Therefore, there are the case where the control parameters need to be changed within a large range to obtain different control effects,



Fig. 16. The simulation results of parallel operation. (a) converters with equal capacity. (b) converters with unequal capacity.

and the case where the control effects change greatly when control parameters change with a small interval. Besides, it is proved that the bi-DC converter control system can still maintain stability even if the parameter changes in a large range.

## C. Multi-Parallel Operation of bi-DC Converters

In order to verify the effectiveness of the proposed inertia matching method, simulation analysis is performed for parallel systems with the same capacity and different capacities.  $P_{\rm const}$  increases by 500 W at 1.5 s and decreases by 500 W at 3.0 s. The simulation results are shown in Fig. 16. In Fig. 16(a),  $R_{\rm d}$  and  $J_{\rm vir}$  are selected in a 1:1 ratio, the load is evenly shared between the bi-DC converters, and the output voltage transition process remains synchronized. Fig. 16(b) shows the case where the load is shared between bi-DC converters in a ratio of 1:2.  $R_{\rm d}$  should be selected according to the ratio of 2:1. At the same time, in order to ensure the synchronization of the output voltage transition process,  $J_{\rm vir}$  should be selected according to the ratio of 2:1.

# VII. CONCLUSION

A VIDC strategy for bi-DC converter is proposed and its essence is connecting a virtual capacitor and a controlled current source in parallel, and a virtual resistance in series on the output side of bi-DC converter, which makes the external characteristics of bi-DC converter consistent with the dynamic characteristics of DC machine. Virtual inertia power and damping power are provided by the ESS without increasing system cost and complexity. Combined with droop control, multi-parallel operation of bi-DC converters can be realized. When using zero-pole distribution to analyse the dynamic performance of the VIDC strategy, it is found that bi-DC converter control system can be equivalent to a 2nd-order model which simplifies the parameter design. Thus, appropriate control parameters can be selected according to the requirements for performance indices, such as damping ratio, overshoot and/or setting time, in 2nd-order system. Based on the inertia matching method,  $J_{vir}$  should be configured according to the capacity ratio to ensure that the output voltage remain synchronized during transient processes. Simulation results show the proposed strategy provides satisfactory inertia and damping effects in DC-MG.

Future work will concentrate on the adaptability of the designed parameters in a wide range of working conditions, and parameter optimization design methods will be studied. The method of suppressing circulating current caused by line resistance will also be focused on.

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