A High Boost Active Switched Quasi-Z-Source Inverter With Low Input Current Ripple

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***Abstract*—This paper deals with a new single-stage high boost quasi-Z-source inverter based on the active switched Z-impedance network. The proposed inverter provides higher voltage boost factor, draws continuous input current, shares the same ground between the input source and the bridge inverter. Compared with the traditional enhanced boost (quasi-)Z-source inverters (EB-ZSI/EB-qZSI), for two less inductors, one less capacitor and one additional active switch used at the impedance network, the output voltage boost factor of the proposed inverter is twice as much as the EB-ZSI and EB-qZSI, which implies that it can use a very higher modulation index to provide improved quality output waveforms. Besides, for obtaining the same dc-ac output voltage gain, the proposed method has lower active switching voltage stress, lower passive component voltage ratings and lower shoot-through current stress with lower input current ripple. The operation theory analysis, power loss calculation, simulation results and performance comparison with other high boost impedance source inverters are presented. To verify the operating theory of the proposed inverter, a laboratory prototype based on the TMS320F28335 DSP was constructed and tested with 60V dc input and ac 110Vrms phase output. Finally, both simulations and the experimental results confirmed that the proposed inverter has high boost voltage inversion capability.**

***Index Terms*—High voltage gain, voltage boost factor, impedance network, quasi-Z-source inverter (qZSI), shoot-through state, switched-boost inverter (SBI).**

I. INTRODUCTION

THE original Z-source inverter (ZSI) was firstly designed by Peng [1] in 2003. It has a two-port impedance network that cascaded between the main bridge inverter and the input voltage source. This novel Z-source network is composed of two capacitors, one diode and two inductors, as shown in Fig. 1(a). Unlike the traditional voltage source inverters (VSIs), the ZSI can achieve both boost and buck capabilities with one single power conversion stage[2]. Two power switches in one phase leg can be turned on at the same time, and there is no need to insert dead time to control the bridge inverter, so the whole inverter system's reliability and the output waveform quality can be further improved. Therefore, the study of ZSIs has became a hot research topic in recent years [3]-[32] due to the flexibility of these classical topologies. In [6]-[8], quasi-Z-source inverters (qZSIs) were presented to overcome the drawbacks of the traditional ZSI, as shown in Fig. 1(b), which have the following advantages such as lower passive component ratings, continuous input current and joint same ground between the main bridge inverter and the input source. However, the voltage boost factor of these qZSIs are still same as the original ZSI, which are not very enough for a lot of high boost industrial applications.

Recently, in order to ameliorate the output waveform of ZSIs by using a very high modulation index, many new high boost inverter topologies based on the Z-network have been proposed [9]-[31]. By adding extra passive and active (capacitors, inductors, diodes) components into the quasi-Z-source network, extended boost-qZSIs (CA-qZSIs/DA-qZSIs) were put forward in [9]. Combining the switched-capacitor(SC) and switched-inductor(SL) structures with the (quasi-) Z-source networks, SL-ZSI in [10], SL-qZSIs in [11]-[12] and generalized multicell SL/SC-ZSIs [13] were proposed, respectively, which can also provide higher output voltage gain than the classical (q)ZSIs. Moreover, by using the enhanced boost (quasi-)Z-source network to replace the traditional qZS network, two new types of EB-ZSI [14] and EB-qZSI [15] were presented, respectively, as shown in Fig. 2, which possess a very high voltage boost factor than the other cascaded boost ZSIs, but at the cost of too many inductors and capacitors used at the impedance network. Thus, in order to produce higher voltage gain with fewer number of components, transformers and coupled-inductors are applied to replace the traditional inductors in the qZS networks. Then, trans-ZSI [16], Γ-ZSI [17], YSI [18] and other new magnetically coupled impedance source inverters [19] have been put forward, respectively. Although they can produce higher-gain voltage, the output dc-link voltage is sensitive to the leakage inductance of coupled inductors and will has voltage spikes superimposed on it.

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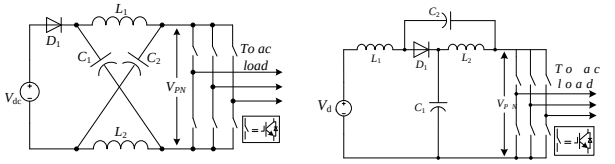
In [20] and [21], switched boost inverters (SBIs) were designed based on the inverse Watkins–Johnson topology. In order to ameliorate the output voltage gain and the input current profile, a class of quasi-SBIs (qSBIs) were proposed in [22] and [23]. Compared with the classical qZSI, the qSBI can provide the same features as ZSI/qZSI, but with a less number of passive elements and one extra switch used at the impedance network, and has higher efficiency [24]. By using one SL cell to replace the inductor in the qSB network, a series of high boost SL-qSBIs were presented in [25]-[27], but with high voltage stress on passive and active components, the input current ripple is also high. Similarly, by applying the SC-cells into the qSB network, high boost SC-qSBIs were proposed in [28]. In [29]-[30], another two new high-gain voltage switched qZSIs with less passive components was proposed, but the input voltage source doesn't share the same ground with the inverter bridge. To address this problem, a common grounded EB-qZSI with an active switched Z-network (EB-ASqZSI) [31] was proposed, which has the same voltage boost factor as that of HG-qSBI [30].

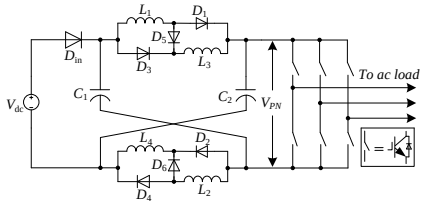
In this paper, by combining with a new active switched Z-impedance network, a non-coupled inductor type qZSI is constructed, as presented in Fig. 3. In comparison to the conventional EB-ZSI[14]/EB-qZSI[15], by using two less inductors, one less capacitor and an additional power switch at the impedance network, the output voltage gain of the proposed inverter is twice as much as the EB-ZSI/EB-qZSI. In addition, the proposed topology has improved input current profiles, shares same ground between the bridge inverter and the input voltage source, has lower passive and active component voltage ratings, lower shoot-through current stress, and can suppress the inrush startup current, which would be suitable for the renewable power generation systems.

The remainder of this paper is organized as follows. Steady state operating principle analysis and the boost factor derivation is presented in Section II. It is followed by the parameter design guidelines in Section III. In Section IV and V, small-signal analysis and characteristics comparison with other high boost inverters are presented, respectively. In Section VI, simulation and experimental verifications are conducted. Finally, Section VII draws the conclusion part.

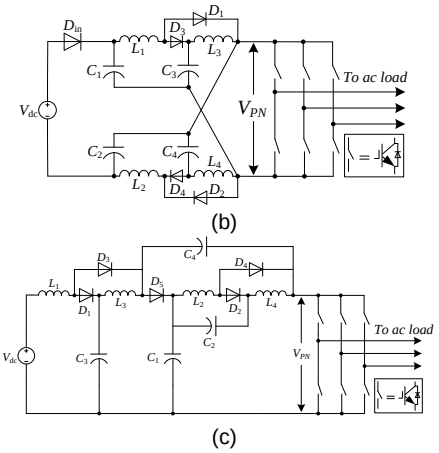


(a) (b)

Fig. 1. Classical (quasi-)Z-source inverters: (a) Original ZSI [1], (b) quasi-ZSI [6].



(a)



(b)

(c)

Fig. 2. The well-known traditional high step-up non-isolated qZSIs: (a) SL-ZSI [10], (b) Enhanced boost-ZSI (EB-ZSI) [14], (c) Enhanced boost-qZSI (EB-qZSI) [15].

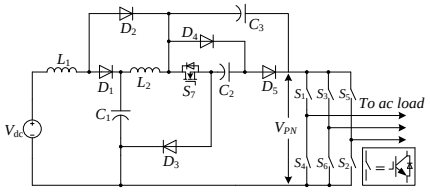


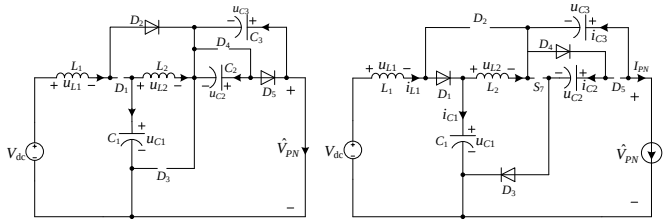
Fig. 3. Proposed high boost non-isolated qZSI with an active switched Z-impedance network.

II. Operating Principle of The Proposed Inverter

The steady-state operating theory analysis and derivation of capacitor voltages and the output voltage boost factor will be presented in this part. For simplification, all the active and passive devices are assumed to be lossless in this section.

A. Steady-state Operating Principle Analysis

Similar to traditional impedance-source inverter topologies, for the sake of analysis, the operating modes of the proposed inverter can be simplified as non-shoot-through state (i.e. traditional two zero states and six active states) and shoot-through state. Thus, the equivalent circuit schematic diagrams of the proposed topology during these two operating states are depicted in Fig. 4. In addition, the inverter's dc side theoretical operational waveforms are presented in Fig. 5.



(a) (b)

Fig. 4. Equivalent circuits of the proposed inverter. (a) Shoot-through state and (b) non-shoot-through state.

1) Shoot-Through State: All the power switches from S_1 to S_7 are conducted at the same time, as shown in Fig. 4(a), and the inverter bridge operates in the short circuit mode. During this state, diodes D_1, D_3, D_4 are reverse-biased, diodes D_2 and D_5 are forward-biased. The input voltage source V_{dc} and capacitor C_2 discharge the energy to inductor L_1. Capacitor C_1 and C_2 discharge the energy to inductor L_2. Due to capacitor C_3 is

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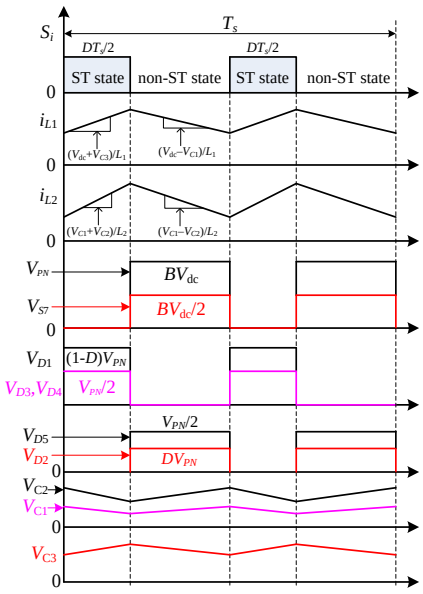

Fig. 5. The dc side theoretical waveforms of the proposed inverter.

connected in parallel with capacitor C_2, then, C_3 is charged by C_2. Thus, the capacitor voltage V_{C3} is equal to V_{C2}, i.e., V_{C3}=V_{C2}. The time interval of this mode is $D \cdot T_s$, where D is shoot-through duty cycle of the inverter bridge during one switching period, T_s. By applying KVL and KCL to Fig. 4(a), the following equations can be derived as

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = V_{dc} + V_{C2} \\ L_2 \dfrac{di_{L_2}}{dt} = V_{C1} + V_{C2} \\ \hat{V}_{PN} = 0 \end{cases} \quad \text{and} \quad \begin{cases} C_1 \dfrac{du_{C_1}}{dt} = -I_{L_2} \\ C_2 \dfrac{du_{C_2}}{dt} + C_3 \dfrac{du_{C_3}}{dt} = -I_{L_1} - I_{L_2} \end{cases} \tag{1}$$

2) Non-Shoot-Through State: During this state, the extra switch S_7 is turned off, and the three-phase inverter bridge operates in either active or zero states. The diodes D_1, D_3, D_4 are turned on, while diodes D_2 and D_5 are reverse-blocking. Inductor L_1 and V_{dc} discharge the energy to C_1. Capacitor C_2 is charged by inductor L_1, L_2 and V_{dc}. Due to the large capacitance values of capacitors (C_1, C_2, C_3) and the high switching frequency, the capacitor voltages u_C can be assumed to be constant. Therefore, in this operating state, V_{C3} is still assumed to be equal to V_{C2}, i.e., V_{C3}=V_{C2}. Meanwhile, inductors L_1, L_2 and capacitor C_3 connect in series with V_{dc} to transfer the stored energy to the ac load side. The time interval of this operating mode is (1-D) T_s. By applying KVL and KCL, one can obtain

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = V_{dc} - V_{C_1} \\ L_2 \dfrac{di_{L_2}}{dt} = V_{C_1} - V_{C_2} \\ \hat{V}_{PN} = V_{C2} + V_{C3} \end{cases} \quad \text{and} \quad \begin{cases} C_1 \dfrac{du_{C_1}}{dt} = I_{L_1} - I_{L_2} \\ C_2 \dfrac{du_{C_2}}{dt} = I_{L_2} - I_{PN} \\ C_3 \dfrac{du_{C_3}}{dt} = -I_{PN} \end{cases} \tag{2}$$

B. Derivation of the Voltage Boost Factor

Based on the volt-second balance property of inductors L_1 and L_2, the average inductors' voltage in steady state over one switching period T_s is zero. Thus, from (1) to (2), we have

$$D(V_{dc} + V_{C2}) + (1-D)(V_{dc} - V_{C1}) = 0 \tag{3}$$

$$D(V_{C1} + V_{C2}) + (1-D)(V_{C1} - V_{C2}) = 0 \tag{4}$$

From (1)-(4), the capacitor voltages and peak dc-link voltage of the proposed topology can be derived as

$$V_{C1} = \frac{1-2D}{1-4D+2D^2} V_{dc} \quad V_{C2} = V_{C3} = \frac{1}{1-4D+2D^2} V_{dc} \tag{5}$$

$$V_{S7} = V_{C2} = \frac{1}{1-4D+2D^2} V_{dc} \tag{6}$$

$$\hat{V}_{PN} = V_{C2} + V_{C3} = \frac{2}{1-4D+2D^2} V_{dc} \tag{7}$$

Similarly, based on the ampere-second balance principle of capacitors C_1, C_2 and C_3, one can obtain

$$I_{L1} = \frac{2(1-D)}{1-4D+2D^2} I_{PN} \quad I_{L2} = \frac{2(1-D)^2}{1-4D+2D^2} I_{PN} \tag{8}$$

where I_{PN} is corresponding the average dc-link current, I_{PN}= (1-D)V_{PN}/R_l, R_l is the simplified equivalent dc load of the ac side circuit [30].

From (7), the voltage boost factor of the proposed inverter can be obtained as

$$B = \frac{\hat{V}_{PN}}{V_{dc}} = \frac{2}{1-4D+2D^2} \qquad D \in (0,\ 0.293) \tag{9}$$

where the operating range of the shoot-through duty cycle D is limited to 0<D<0.293. In addition, when D equals to zero, the corresponding voltage boost factor B is one instead of two, which is determined by the internal structure of the power circuit. However, when D is between 0 and 0.293, the produced boost factor will be identical to that of (9).

Based on (9), Fig. 6 shows the voltage boost factor B comparison between the proposed scheme and the other eight traditional high boost impedance source inverters (EB-qZSI [15], SL-ZSI [10], EB-ZSI [14], ASC/SL-qZSI[25]/rSL-qSBI [26] (with two SL-cells), SC-qSBIs [28] and the EB-ASqZSI [31]). Accordingly, it can be found from Fig. 6 that the output voltage boost factor of the proposed topology is two times as much as the EB-ZSI/EB-qZSI, and much higher than that of the SL-ZSI, SC-qSBIs and the EB-ASqZSI during the whole shoot-through duty cycle range. Compared with the ASC/SL-qZSI and rSL-qSBI, the proposed inverter can also produce higher boost factor when 0<D<0.202.

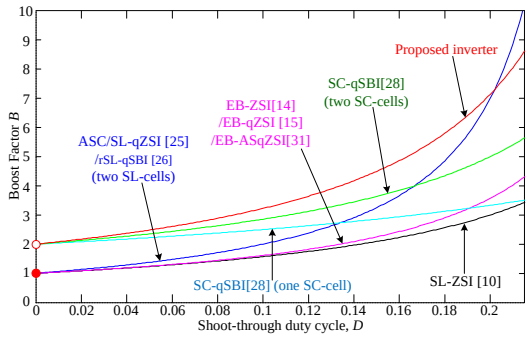

Fig. 6. Voltage boost factor B comparison for these high boost inverters.

III. Parameters Design of The Impedance Network

Generally, the active and passive elements' parameter design of a converter mainly depends on their rated currents and rated voltages, respectively, which have been summarized in Table I.

A. Inductance Selection

Based on the steady-state operating theory analysis in Section II-A, from (1), the peak-to-peak inductor current ripples of i_{L1} and i_{L2} can be derived as

$$\Delta i_{L1}=\frac{V_{dc}+V_{C2}}{L_1}DT_L \qquad \Delta i_{L2}=\frac{V_{C1}+V_{C2}}{L_2}DT_L \tag{10}$$

where T_L=1/f_L, and f_L is the operating frequency of inductor currents (i_{L1}, i_{L2}). From Fig. 5, it can be observed that the operating frequency f_L of i_{L1} and i_{L2} is two times that of the switching frequency f_s, i.e., f_L=2f_s.

Substituting (5)-(9) into (10), the inductance values of L_1 and L_2 can be designed by

$$L_1=\frac{D\left(2-4D+2D^2\right)R_l}{4x_{L1}\%\left(1-D\right)^2Bf_s} \qquad L_2=\frac{D\left(1-4D+2D^2\right)R_l}{4x_{L2}\%\left(1-D\right)^2f_s} \tag{11}$$

where x_{L1}%=$\Delta i_{L1}/I_{L1}$, x_{L2}%=$\Delta i_{L2}/I_{L2}$ are the maximum permitted fluctuation range of inductor currents.

B. Capacitance Selection

Similarly, from (2), the peak to peak capacitor voltage ripples of C_1, C_2 and C_3 can be obtained as

$$\Delta u_{C1}=(1-D)T_L\left(I_{L1}-I_{L2}\right)/C_1 \tag{12}$$

$$\Delta u_{C2}=\frac{I_{L2}-I_{PN}}{C_2}(1-D)T_L \qquad \Delta u_{C3}=\frac{I_{PN}}{C_3}(1-D)T_L \tag{13}$$

Substituting the expressions of (5) and (8) into (12)-(13), the capacitances of C_1, C_2 and C_3 can be calculated by

$$C_1=\frac{D\left(1-D\right)^3B}{x_{C1}\%\left(1-2D\right)R_lf_s} \qquad C_2=\frac{\left(1-D\right)^2B}{2x_{C2}\%R_lf_s} \qquad C_3=\frac{\left(1-D\right)^2}{x_{C3}\%R_lf_s} \tag{14}$$

where x_{C1}%=$\Delta u_{C1}/V_{C1}$, x_{C2}%=$\Delta u_{C2}/V_{C2}$ and x_{C3}%=$\Delta u_{C3}/V_{C3}$ are the maximum permitted capacitor voltages' fluctuation range of V_{C1}, V_{C2} and V_{C3}, respectively.

C. Parameters selection of Active Switching Devices

Normally, the parameter types of the active power switch S_7 and diodes can be selected based on their current and voltage stresses, respectively, as tabulated in Table I.

TABLE I
Voltage and Current Stresses of The Proposed Topology

Proposed inverter			
Parameter	Voltage Stress	Parameter	Current Stress
C_1	$\frac{1-2D}{1-4D+2D^2}V_{dc}$	L_1	$\frac{2(1-D)}{1-4D+2D^2}I_{PN}$
C_2, C_3	$\frac{1}{1-4D+2D^2}V_{dc}$	L_2	$\frac{2(1-D)^2}{1-4D+2D^2}I_{PN}$
D_1	$\frac{2(1-D)}{1-4D+2D^2}V_{dc}$	D_1, D_2	$\frac{2(1-D)}{1-4D+2D^2}I_{PN}$
D_2	$\frac{2D}{1-4D+2D^2}V_{dc}$	D_3, D_4	$\frac{1}{1-4D+2D^2}I_{PN}$
D_3, D_4, D_5	$\frac{1}{1-4D+2D^2}V_{dc}$	D_5	$\frac{1-D}{D(1-4D+2D^2)}I_{PN}$
S_7	$\frac{1}{1-4D+2D^2}V_{dc}$	S_7	$\frac{1-D}{D(1-4D+2D^2)}I_{PN}$

IV. Small-Signal Dynamic Analysis of The Proposed Inverter

To simplify the analysis, the ac-side circuit of the proposed qZSI is represented by its simplified equivalent dc load [23], as shown in Fig. 7. This equivalent dc inductive load (Z_l=R_{ld}+sL_{ld}) is directly connected in parallel with an active power switch S_i, where v_{ld} and i_{ld} are the instantaneous load voltage and current, respectively.

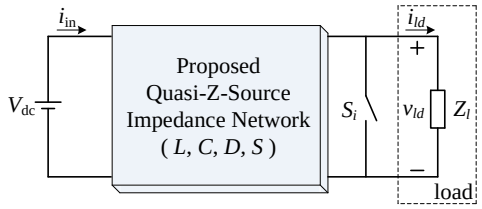

Fig. 7 Simplified and unified equivalent circuit of the proposed qZS inverter.

By using the similar small-signal analysis method in [23], and after Laplace transformation, the control-to-capacitor voltage transfer function can be derived in (A1), and the detailed derivation is presented in Appendix.

Based on (A1), Fig. 8 shows the theoretical bode plots of the proposed qZSI for the inductive load. The parameters are L_1=L_2=L=1mH, C_1=C_2=C_3=C=470uF, R_{ld}=5Ω and L_{ld}=1mH. From Fig. 8, it can be observed that the slope inclination is about -20dB/dec on the crossing frequency, and all the poles of these two transfer functions are all lied on the left side of the s plane, which indicates that the stability of this open loop system can be guaranteed.

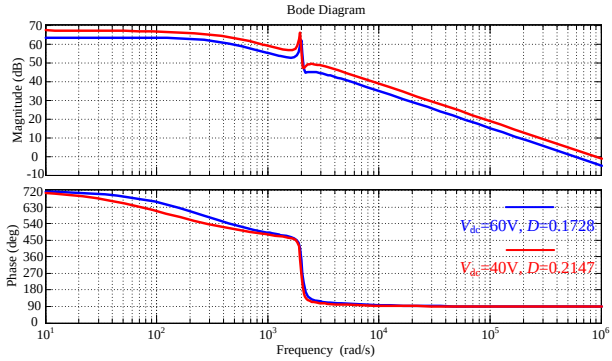

Fig. 8 Bode plots of the control-to-capacitor voltage transfer function of the proposed inverter when V_{dc}=60V, D=0.1728 and V_{dc}=40V, D=0.2147.

V. Characteristics Comparison With Other High Boost Impedance Source Inverters

A. Comparison of Devices Count

The comparison of the number of passive and active elements used in the SL-ZSI, EB-ZSI/EB-qZSI, ASC/SL-qZSI, rSL-qSBI, SC-qSBI, EB-ASqZSI and the proposed scheme is tabulated in Table II. Compared with the SL-ZSI [10], the proposed method uses one more capacitor and one more active power switch, but it has two less inductors and two less diodes. In addition, the proposed topology uses two less inductors, one less capacitor and one extra power switch than the EB-ZSI/EB-qZSI. Compared with ASC/SL-qZSI and rSL-qSBI, the proposed topology uses one less inductor, two more capacitors and three less diodes. Therefore, the total number of passive and active devices used at the proposed impedance source network is 11, which is lower than that of the above five high boost inverters. Although the proposed topology uses one more passive element and one more diode than that of the SC-

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TABLE II
Comparison Of Current and Voltage Stresses For These High Boost Impedance Source Inverters

	SL-ZSI [10]	EB-ZSI [14]	EB-qZSI [15]	EB-ASqZSI [31]	SC-qSBI[28] (two SC-cells)	ASC/SL-qZSI[25] /rSL-qSBI[26] (two SL-cells)	Proposed inverter
Boost Factor (B)	$\frac{1+D}{1-3D}$	$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{2}{1-3D}$	$\frac{1+2D}{1-4D}$	$\frac{2}{1-4D+2D^2}$
Inductor	4	4	4	2	1	3	2
Capacitor	2	4	4	2	3	1	3
Diode/Switch	7/0	5/0	5/0	4/1	4/1	8/1	5/1
Capacitor Voltage Stresses (V_C/V_{dc})	$(1–D)B/(1+D)$	$(1–D)^2B$ $(1–D)B$	$(1–D)^2B$ $D(1–D)B$ $D(2–D)B$ $(1–3D+D^2)B$	B $(1–2D)B$	$B/2$	B	$B/2$ $(1–2D)B/2$
Diode Voltage Stresses (V_D/V_{dc})	B $DB/(1+D)$ $(1–D)B/(1+D)$	B DB $(1–D)B$	B DB $(1–D)B$	B $2DB$ $(1–2D)B$	B $B/2$	B $2DB/(1+2D)$ $2(1–D)B/(1+2D)$	$B/2$ DB $(1–D)B$
Voltage Stress of switch S_7 (V_{S7}/V_{dc})	——	——	——	B	$B/2$	B	$B/2$
Buck-Boost Factor (G=MB)	$\frac{4M-\sqrt{3}M^2}{3\sqrt{3}M-4}$	$\frac{2M}{3M^2-2}$	$\frac{2M}{3M^2-2}$	$\frac{2M}{3M^2-2}$	$\frac{4}{3\sqrt{3}M-4}$	$\frac{3-\sqrt{3}M}{2\sqrt{3}M-3}$	$\frac{4M}{3M^2-2}$
Inductor Current Stresses (I_L/I_{PN})	$(1–D)B/(1+D)$	$(1–D)B$ $(1–D)^2B$	$(1–D)B$ $(1–D)^2B$	$(1–D)B$ $(1–D)^2B$	$(1–D)B$	$(1–D)B/(1+2D)$	$(1–D)B$ $(1–D)^2B$
Input Current	0; $2I_{L1}$-I_{PN}	0; $2I_{L1}$-I_{PN}	I_{L1}	I_{L1}	I_{L1}	I_{L1}; $3I_{L1}$	I_{L1}
Shoot-through Current Stresses (I_{sh}/I_{PN})	$4(1–D)B/(1+D)$	$2(1–D)B+2(1–D)^2B$	$2(1–D)B+2(1–D)^2B$	$(1–D)B+(1–D)^2B$	$(1–D)B$	$3(1–D)B/(1+2D)$	$(1–D)B+(1–D)^2B$
Common Ground	No	No	Yes	Yes	Yes	No	Yes
Average DC-link Current (I_{PN})	$\frac{(1-D)\hat{V}_{PN}}{R_l}$	$\frac{(1-D)\hat{V}_{PN}}{R_l}$	$\frac{(1-D)\hat{V}_{PN}}{R_l}$	$\frac{(1-D)\hat{V}_{PN}}{R_l}$	$\frac{(1-D)\hat{V}_{PN}}{R_l}$	$\frac{(1-D)\hat{V}_{PN}}{R_l}$	$\frac{(1-D)\hat{V}_{PN}}{R_l}$

Here, B is the inverter's output voltage boost factor (B=V_{PN}/V_{dc}), R_l is the simplified equivalent dc load of the inverter's ac side circuit.

qSBI (two SC-cells) [28] and the EB-ASqZSI [31], it can produce a very high voltage boost factor than both of them, as shown in Fig. 6.

B. Comparison of Boost Abilities

Fig. 6 has compared the boost factor between the proposed method and other eight inverters. The relationship between the shoot-through duty cycle D and the modulation index M for the maximum constant boost control (MCBC) strategy [33] can be described as $D=1-\sqrt{3}M/2$.

For the three-phase inverter system, its peak ac output phase voltage can be defined as

$$\hat{V}_{ac}=M\cdot\frac{\hat{V}_{PN}}{2}=MB\cdot\frac{V_{dc}}{2}=G\cdot\frac{V_{dc}}{2} \tag{15}$$

where the buck-boost factor G=MB, which can be identified as the dc-ac output voltage gain of the whole inverter system. Therefore, the ideal buck-boost factor G of the proposed topology can be derived as

$$G=MB=\frac{2M}{1-4D+2D^2}=\frac{4M}{3M^2-2} \tag{16}$$

Fig. 9 shows the comparison of modulation index M versus the buck-boost factor G for these high boost inverters. It can be found that the proposed inverter has higher buck-boost factor G through the whole modulation index M range than those of the SL-ZSI, EB-ZSI, SC-qSBIs, EB-qZSI and the EB-ASqZSI. Therefore, the proposed topology can use higher modulation index M and lower shoot-through duty cycle D to produce the same dc-ac output voltage gain G, which implies that lower components' voltage ratings and better output waveforms' quality can be achieved.

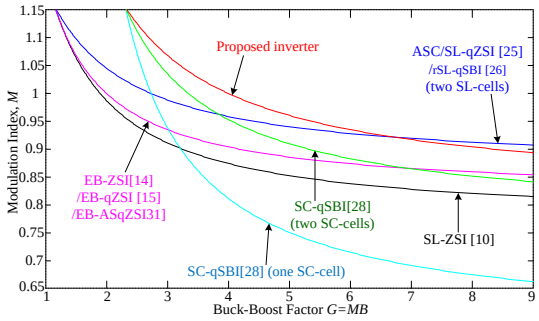

Fig. 9. Plot of modulation index M versus the buck-boost factor G.

C. Comparison of Current and Voltage Stresses

For these high boost inverter topologies, their corresponding

current and voltage stresses of the active and passive components are summarized in Table II. Based on Table II, the comparison of capacitor voltage stress is depicted in Fig. 10(b). From this figure, it can be seen that for obtaining the same dc-ac output voltage gain G, the proposed converter has lower capacitor voltage stress than ASC/SL-qZSI, SC-qSBIs, EB-AS qZSI, SL-ZSI, rSL-qSBI, and the EB-ZSI. The inductor current stress comparison between the proposed inverter and the other inverter topologies is presented in Fig. 10(a). From Fig. 10(a), the proposed topology has a little higher inductor current stress than the SL-ZSI, rSL-qSBI, ASC/SL-qZSI, EB-ZSI/EB-qZSI and the EB-ASqZSI, but same as the SC-qSBIs. The shoot-through current stress of the proposed inverter, as presented in Fig. 10(c), is only slightly higher than the EB-ASqZSI and the SC-qSBIs, but much lower than those of the rSL-qSBI, EB-ZSI, ASC/SL-qZSI, EB-qZSI and the SL-ZSI.

The active switching voltage stress across the power switches can be described as the ratio of the peak switching voltage (V_{PN}, V_{S7}) to an equivalent dc voltage $GV_{\rm dc}$, as defined in [33], which can be expressed as

$$\frac{\hat{V}_{PN}}{GV_{dc}}=\frac{BV_{dc}}{GV_{dc}}=\frac{2G}{1+\sqrt{2G^2+1}} \qquad \frac{V_{S_7}}{GV_{dc}}=\frac{G}{1+\sqrt{2G^2+1}} \tag{17}$$

Based on (17), Fig. 10(d) compares the active switching voltage stress across the extra switch S_7 and the main bridge inverter. From Fig. 10(d), one can find that the inverter bridge's switching voltage stress of the proposed topology is lower than the SC-qSBIs, SL-ZSI, EB-ZSI, EB-ASqZSI and the EB-qZSI. Although it is slightly higher than that of the ASC/SL-qZSI and rSL-qSBI (two SL-cells) when G is higher than 6, the voltage stress of the active switch S_7 is much lower than those of the other eight inverter topologies.

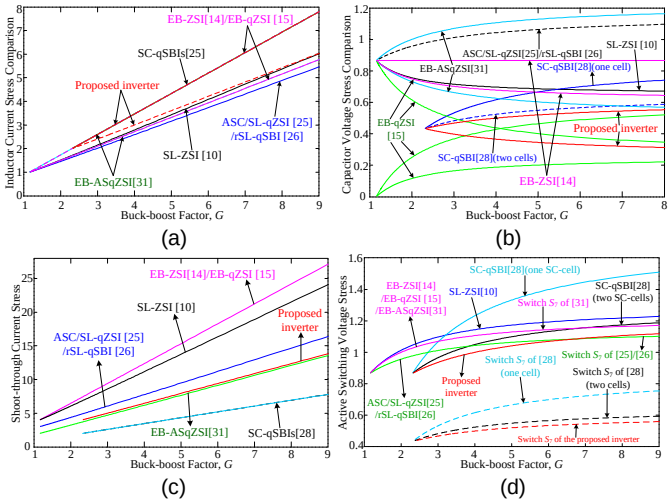

Fig. 10. Current and voltage stress comparison: (a) Comparison of inductor current stresses, (b) Comparison of capacitor voltage stresses, (c) Shoot-through current stresses comparison, (d) Comparison of active switching voltage stresses.

In order to better quantify the current and voltage stresses of active switching elements (MOSFETs/diodes) in the proposed converter system, the peak and average switching device power (SDP) are computed and compared with other high step-up (q)ZSIs in the following. The SDP of an active semiconductor device can be expressed as the product of its current and voltage stresses [2]. The total SDP for a whole converter system can be defined as the summation of SDP of all the active switching elements used in the circuit, which is a good cost indicator for a given inverter system.

The peak and average SDP of MOSFETs and diodes for the proposed inverter are derived as

$$\begin{cases} SDP_{(pk\_MOS)}=SDP_{(peak\_inverter)}+SDP_{(peak\_S_7)} \\ \quad =\max\left[\dfrac{4(2-D)}{1-4D+2D^2}+\dfrac{4}{\cos\phi M},\ \dfrac{8}{\cos\phi M}\right]P_o+\dfrac{P_o}{2D(1-4D+2D^2)} \\ SDP_{(pk\_diodes)}=\dfrac{5D-4D^2+1}{2D(1-D)(1-4D+2D^2)}P_o \end{cases} \tag{18}$$

$$\begin{cases} SDP_{(av\_MOSFETs)}=SDP_{(av\_inverter)+(av\_S_7)}=\dfrac{8D-4D^2+0.5}{1-4D+2D^2}P_o+\dfrac{8(1-D)}{\cos\phi\pi M}P_o \\ SDP_{(av\_diodes)}=\dfrac{4D^2-4D+3.5}{1-4D+2D^2}P_o \end{cases} \tag{19}$$

Based on (18) and (19), Fig. 11 shows the average and peak SDP comparison of active switching devices (diodes and MOSFETs) for these high boost impedance source inverters. From Fig. 11(a) to Fig. 11(f), it can be found that the diodes' average and peak SDP, MOSFETs' average and peak SDP of the proposed inverter are all much lower than the EB-ASqZSI [31], EB-ZSI [14], ASC/SL-qZSI (two SL-cells) [25], EB-qZSI [15], rSL-qSBI (two SL-cells) [26] and the SL-ZSI[10], but slightly higher than that of the SC-qSBIs [28].

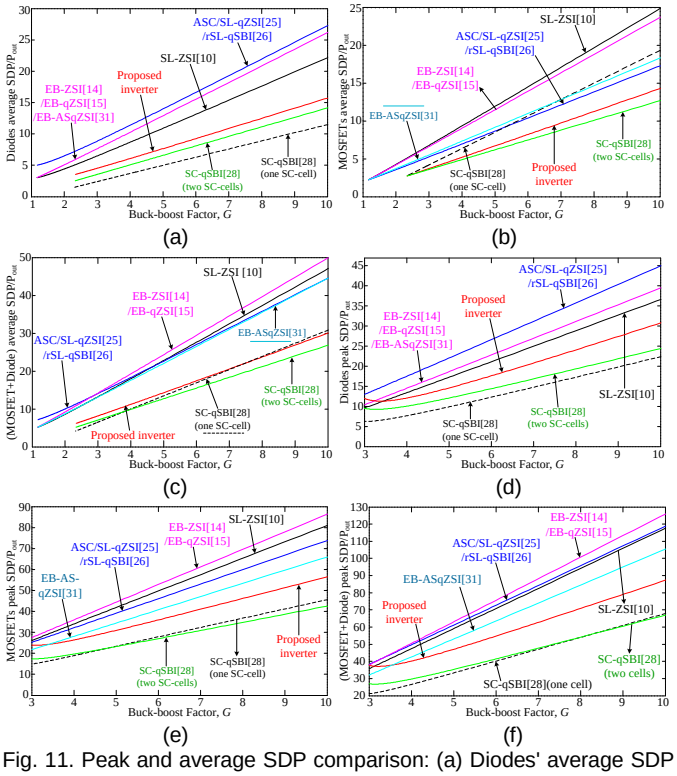

Fig. 11. Peak and average SDP comparison: (a) Diodes' average SDP comparison, (b) MOSFETS' average SDP comparison, (c) Total average SDP (MOSFETs+diodes) comparison, (d) Diodes' peak SDP comparison, (e) MOSFETS' peak SDP comparison, (f) Total peak SDP (MOSFETs+diodes) comparison.

D.Input Current Ripple Comparison

The input current ripples of the power converters are varied with different control conditions. For clearly comparison, the inductor current ripples for all the inverters are assumed to be small and insignificant. The MCBC control method was

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applied to analyze the characteristics of the input current ripple for all the compared topologies. And the ac-side circuit of the inverters is represented by a simplified equivalent dc load [30].

For the classical SL-ZSI [10], the input current is the current flow through diode D_{in}. In ST state, the input current is zero; while, in the non-ST state, the input current is $2I_L$-I_{PN}. Hence, the average input current of the SL-ZSI is $(1+D)I_L$.

The detailed input current for the SL-ZSI is shown in Fig. 12(a). Then its corresponding input current ripple can be derived as

$$\Delta I_{in_1} = \left| i_{in} - (1+D) I_L \right| = \left| (1-D) I_L - I_{PN} \right| \tag{20}$$

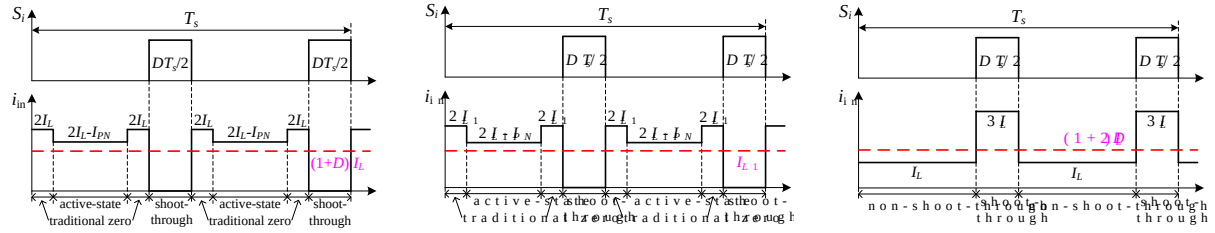
For the EB-ZSI [14], the corresponding input current is the current flow through diode D_{in}. The input current in the ST state is zero; while, in the non-ST state, the input current is $2I_{L1}$-I_{PN}. Then, the corresponding average input current value of EB-ZSI is I_{L1}. The detailed input current profile for the EB-ZSI is shown in Fig. 12(b). The deviation between the average value and the input current can be expressed by

$$\Delta I_{in_2} = \left| i_{in} - I_{L1} \right| = \left| (1-2D) I_{L1} - I_{PN} \right| \tag{21}$$

For the two SL-cells' ASC/SL-qZSI [25] and rSL-qSBI [26], the input current in ST state is $3I_L$ and the input current in non-ST state is I_L. Thus, the corresponding average input current is $(1+2D)I_L$. And the detailed input current for the ASC/SL-qZSI and rSL-qSBI is shown in Fig. 12(c). And its input current ripple can be derived as

$$\Delta I_{in_3} = \left| i_{in} - (1+2D) I_L \right| = \left| 2D I_L \right| \tag{22}$$

For the proposed inverter, the input current is the current flow through inductor L_1, which is same as the EB-qZSI [15], EB-ASqZSI [31] and the SC-qSBIs [28]. Therefore, the input current ripple for these four high boost inverters are negligible and can be assumed to be zero. Table II also shows the input current profiles for all these inverter topologies. As a result, compared with (20)-(22), the input current ripple of the proposed converter is lower than those of the SL-ZSI [10], ASC/SL-qZSI [25], EB-ZSI [14] and the rSL-qSBI [26], but same as EB-qZSI [15], EB-ASqZSI [31] and SC-qSBIs [28].



(a) (b) (c)

Fig. 12 Input current ripples of (a) SL-ZSI [10], (b) EB-ZSI [14], (c) ASC/SL-qZSI [25] and rSL-qSBI (two SL-cells) [26].

E. Power Loss Calculation and Efficiency Comparison

For the proposed inverter, the total power loss consists of inductor loss, capacitor loss, active power MOSFET loss and diode loss, which will be calculated in detail in the following, respectively.

1) Inductor Power Loss

The inductor's power loss consists of the winding copper loss and core loss. However, when compared with the total copper conduction loss, the core loss is very small and can be negligible, which is due to the small inductor current ripples. The winding copper loss mainly depends on the winding copper resistance and the RMS current value flowing through it. From (8), the approximate RMS value of the inductor currents can be derived as

$$I_{L1(\mathrm{RMS})} = \frac{2(1-D)}{1-4D+2D^2} I_{PN} \quad I_{L2(\mathrm{RMS})} = \frac{2(1-D)^2}{1-4D+2D^2} I_{PN} \tag{23}$$

Thus, the total inductor power loss can be expressed as

$$P_{rL\_loss} = I_{L1(\mathrm{RMS})}^2 r_L + I_{L2(\mathrm{RMS})}^2 r_L = \left(2-2D+D^2\right) r_L \frac{3G^2 \cos\phi}{8|Z_L|} P_{out} \tag{24}$$

where r_L is internal resistance of inductors, the ac load side power factor is cosϕ, Z_L=R_L+jwL_L is the ac resistive-inductive load, and P_{out} is the output power of whole inverter system.

2) Capacitor Power Loss

The capacitor current during ST and non-ST states can be obtained from Fig. 4(a) and Fig. 4(b) as,

$$i_{C1} = \begin{cases} \dfrac{-2(1-D)^2}{1-4D+2D^2} I_{PN} & (0, DT_s) \\ \dfrac{2D(1-D)}{1-4D+2D^2} I_{PN} & (DT_s, T_s) \end{cases} \tag{25}$$

$$i_{C2} = \begin{cases} \dfrac{-(1-D)}{D\left(1-4D+2D^2\right)} I_{PN} & (0, DT_s) \\ \dfrac{1}{1-4D+2D^2} I_{PN} & (DT_s, T_s) \end{cases} \quad i_{C3} = \begin{cases} \dfrac{1-D}{D} I_{PN} & (0, DT_s) \\ -I_{PN} & (DT_s, T_s) \end{cases} \tag{26}$$

Based on (25) and (26), the approximate RMS value of capacitor currents can be derived as

$$I_{C1(\mathrm{RMS})} = \frac{2(1-D)\sqrt{D(1-D)}}{1-4D+2D^2} I_{PN} \tag{27}$$

$$I_{C2(\mathrm{RMS})} = \frac{\sqrt{(1-D)/D}}{1-4D+2D^2} I_{PN} \qquad I_{C3(\mathrm{RMS})} = \sqrt{(1-D)/D} I_{PN} \tag{28}$$

Assuming that the capacitor's equivalent series resistance (ESR) is r_C. Then, the total capacitor conduction power loss is

$$\begin{aligned} P_{rC\_loss} &= I_{C1(\mathrm{RMS})}^2 r_C + I_{C2(\mathrm{RMS})}^2 r_C + I_{C3(\mathrm{RMS})}^2 r_C \\ &= \left[D(1-D) + \frac{1+4/B^2}{4D(1-D)} \right] r_C \frac{3G^2 \cos\phi}{8|Z_L|} P_{out} \end{aligned} \tag{29}$$

where B is the inverter's output voltage boost factor, B= 2/(1-4D+2D^2).

3) Diode Power Loss

The diode power loss is consisted of reverse recovery loss and conduction power loss. The total reverse recovery loss of diodes is $P_{rrD} = 5 \cdot Q_{rr} \cdot \hat{V}_{PN} \cdot f_s$, where Q_{rr} is the diode's reverse

recovery charge, f_s is switching frequency.

Based on the operating theory analysis in Fig. 4, the average and RMS values of diode currents can be derived as

$$\begin{cases} I_{D1(\mathrm{AVG})}=\dfrac{2(1-D)^2}{1-4D+2D^2}I_{PN} \quad I_{D1(\mathrm{RMS})}=\dfrac{2(1-D)\sqrt{1-D}}{1-4D+2D^2}I_{PN} \\ I_{D2(\mathrm{AVG})}=\dfrac{2D(1-D)}{1-4D+2D^2}I_{PN} \quad I_{D2(\mathrm{RMS})}=\dfrac{2(1-D)\sqrt{D}}{1-4D+2D^2}I_{PN} \\ I_{D3,4(\mathrm{AVG})}=\dfrac{1-D}{1-4D+2D^2}I_{PN} \quad I_{D3,4(\mathrm{RMS})}=\dfrac{\sqrt{1-D}}{1-4D+2D^2}I_{PN} \\ I_{D5(\mathrm{AVG})}=\dfrac{1-D}{1-4D+2D^2}I_{PN} \quad I_{D5(\mathrm{RMS})}=\dfrac{\sqrt{D}(1-D)}{D\left(1-4D+2D^2\right)}I_{PN} \end{cases} \tag{30}$$

Then, the power loss associated with the forward voltage drop V_F is

$$\begin{aligned} P_{V_F\_loss}&=I_{D1(\mathrm{AVG})}V_F+I_{D2(\mathrm{AVG})}V_F+2I_{D3(\mathrm{AVG})}V_F+I_{D5(\mathrm{AVG})}V_F \\ &=\frac{5(1-D)}{1-4D+2D^2}V_F I_{PN}=2.5\frac{V_F}{V_{dc}}P_{out} \end{aligned} \tag{31}$$

The ohmic power loss associate with the forward resistance r_D of diodes is

$$\begin{aligned} P_{r_D\_loss}&=I_{D1(\mathrm{RMS})}^2 r_D+I_{D2(\mathrm{RMS})}^2 r_D+2I_{D3(\mathrm{RMS})}^2 r_D+I_{D5(\mathrm{RMS})}^2 r_D \\ &=\frac{6-4D+(1-D)/D}{4(1-D)}r_D\frac{3G^2\cos\phi}{8|Z_L|}P_{out} \end{aligned} \tag{32}$$

Therefore, the total diode power loss can be derived as

$$P_{D\_loss}=P_{rrD}+P_{V_F\_loss}+P_{r_D\_loss} \tag{33}$$

4) MOSFET Power Loss

Generally, the power loss of MOSFET can be divided into conduction power loss and switching power loss during the switching on and off states. From Fig. 4, the current flow through switch S_7 is,

$$i_{S_7}=\begin{cases} \dfrac{1-D}{D\left(1-4D+2D^2\right)}I_{PN} & (0,DT_s) \\ 0 & (DT_s,T_s) \end{cases} \Rightarrow \begin{cases} I_{S_7(\mathrm{AVG})}=\dfrac{1-D}{1-4D+2D^2}I_{PN} \\ I_{S_7(\mathrm{RMS})}=\dfrac{(1-D)\sqrt{D}}{D\left(1-4D+2D^2\right)}I_{PN} \end{cases} \tag{34}$$

Then, the switching power loss and the conduction power loss of switch S_7 is

$$P_{sw7}=\frac{t_{on}+t_{off}}{2}f_{S_7}V_{S_7}i_{S_7}=\left(t_{on}+t_{off}\right)f_s\frac{P_{out}}{2D\left(1-4D+2D^2\right)} \tag{35}$$

$$P_{cond7}=I_{S_7(\mathrm{RMS})}^2 r_{S_7}=\frac{r_{S_7}}{4D}\frac{3G^2\cos\phi}{8|Z_L|}P_{out} \tag{36}$$

where f_s is the switching frequency, t_{on} and t_{off} are the turn-on and turn-off delay times of MOSFETs, r_{S7} is the drain-to-source resistance of switch S_7.

The current flowing through the switches of the bridge inverter can be expressed as

$$i_{S_{inveretr}}=\begin{cases} \dfrac{I_{ST}}{3}=\dfrac{I_{L1}+I_{L2}}{3}=\dfrac{2(1-D)(2-D)}{3\left(1-4D+2D^2\right)}I_{PN} & (0,DT_s) \\ \dfrac{\sqrt{2}P_{out}}{3V_o\cos\phi\pi}=\dfrac{4P_{out}}{3MBV_{dc}\cos\phi\pi} & (DT_s,T_s) \end{cases} \tag{37}$$

Based on (37), the RMS value of the switches' current is

$$I_{S_{inv}(\mathrm{RMS})}=\sqrt{\frac{D}{9}I_{ST}^2+\frac{16(1-D)P_{out}^2}{9\pi^2\cos^2\phi M^2B^2V_{dc}^2}} \tag{38}$$

Then, the switching power loss and the conduction power loss of the bridge inverter are

$$P_{sw\_inverter}=\frac{t_{on}+t_{off}}{2}f_s\hat{V}_{PN}\frac{I_{ST}}{3}\cdot 6=\left(t_{on}+t_{off}\right)f_s\frac{2(2-D)}{1-4D+2D^2}P_{out} \tag{39}$$

$$P_{cond\_inv}=6I_{s_{inv}(\mathrm{RMS})}^2 r_{s\_inv}=\left[\frac{2D(2-D)^2}{3}+\frac{1.08(1-D)}{\cos^2\phi M^2B^2}\right]r_{s\_inv}\frac{3G^2\cos\phi}{8|Z_L|}P_{out} \tag{40}$$

where r_{s_inv} is the parasitic resistance of MOSFETs in the inverter bridge.

Therefore, the total switching power loss and total conduction power loss of all MOSFETs can be derived as

$$P_{sw}=P_{sw7}+P_{sw\_inverter}=\left(t_{on}+t_{off}\right)f_s\frac{4(2-D)+1/D}{2\left(1-4D+2D^2\right)}P_{out} \tag{41}$$

$$\begin{aligned} P_{cond}&=P_{cond7}+P_{cond\_inv} \\ &=\left[\frac{r_{S_7}}{4D}+\left(\frac{2D(2-D)^2}{3}+\frac{1.08(1-D)}{\cos^2\phi M^2B^2}\right)r_{s\_inv}\right]\frac{3G^2\cos\phi}{8|Z_L|}P_{out} \end{aligned} \tag{42}$$

Based on (24), (29), (33), (41)-(42) and the internal parasitic parameters in Table III. The power loss calculation results for these high boost inverters are shown and compared in Fig. 13.

TABLE III
Parasitic Parameters for Power Loss Analysis

Parameters	Values
Parasitic resistance of inductors (L_1, L_2)	0.12Ω
Core of inductors	KS300125A(142nH/N^2)
ESR of capacitors (C_1, C_2 and C_3)	100mΩ
Diodes (RURG3060CC)	600V, 30A, $V_{F(\max)}$=1.3V
MOSFET S_7 (IXFH170N25X3)	250V,170A, $r_{DS\_on(\max)}$=7.4mΩ
MOSFET S_1~S_6 (FCH040N65S3)	650V,65A, r_{DS_on}=35.4mΩ

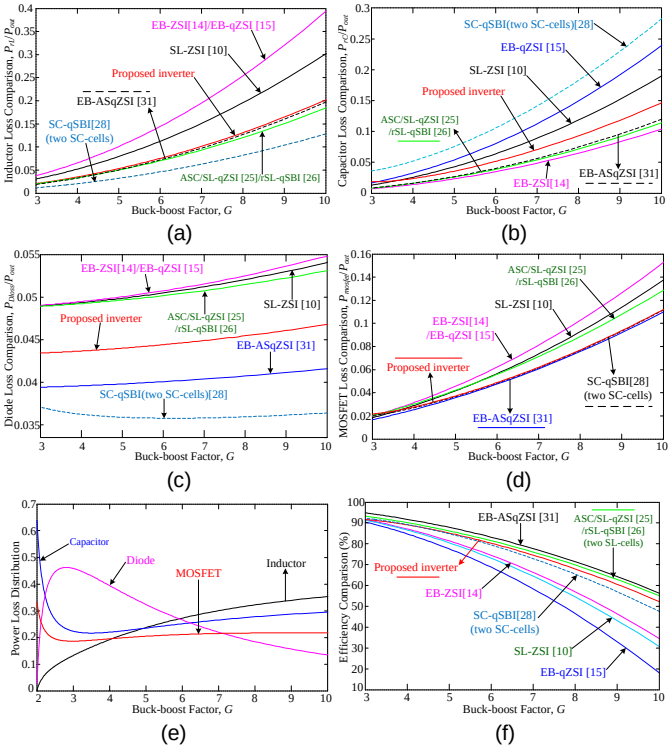


Fig. 13. Power loss analysis and efficiency comparison. (a) Comparison of inductor power loss, (b) Comparison of capacitor power loss, (c) Comparison of diode power loss, (d) Comparison of MOSFET power loss, (e) Loss distribution percentage of the proposed topology, (f) Efficiency comparison.

From Fig.13(a), it can be found the inductor loss of the

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proposed inverter is slightly higher than two SL-cells' ASC/SL-qZSI, rSL-qSBI, SC-qSBI (two SC-cells) and the EB-ASqZSI, but much lower than that of the EB-ZSI, EB-qZSI and SL-ZSI. Fig. 13(b) shows the capacitor loss comparison. From Fig. 13(b), it can be found that the proposed topology has higher capacitor loss than ASC/SL-qZSI, rSL-qSBI, EB-ZSI and the EB-ASqZSI, but lower than the SC-qSBI (two SC-cells), EB-qZSI and the SL-ZSI. The diode and MOSFET power losses comparison are shown in Fig. 13(c) and Fig. 13(d), respectively. From Fig. 13(c), the proposed topology has a higher diode loss than the SC-qSBI and the EB-ASqZSI, but lower than those of the other five inverter topologies (SL-ZSI, EB-ZSI, EB-qZSI, ASC /SL-qZSI and rSL-qSBI). It can be seen that from Fig. 13(d), the proposed topology has lower MOSFET loss than those of the EB-qZSI, rSL-qSBI, SL-ZSI, ASC/SL-qZSI and EB-ZSI, almost same as the SC-qSBI, but slightly higher than the EB-ASqZSI. Fig. 13(e) shows the percentage of the power loss distribution in the proposed topology. Then, it can be found that for obtaining higher dc-ac output voltage gain G, the major power losses come from inductors, capacitors and MOSFETs. Therefore, based on the above power loss analysis (23)-(42) and Table III, the calculated efficiencies for these high boost inverters are compared and plotted in Fig. 13(f). Thus, it can be found from Fig. 13(f) the proposed converter only has a lower efficiency than the EB-ASqZSI, ASC/SL-qZSI and rSL- qSBI (two SL-cells), but higher than those of the other four topologies (EB-ZSI, two SC-cells' SC-qSBI, EB-qZSI and the SL-ZSI).

VI. Simulation and Experimental Verifications

A. Simulation Results

Simulation studies of the proposed inverter are performed based on the MATLAB/Simulink platform. The simulation parameters are selected as: L_1=L_2=1mH, C_1=C_2=C_3=470uF, output filter inductor L_f=2mH, filter capacitor C_f=50uF, the switching frequency of the main inverter bridge is 10kHz, dc input voltage V_{dc}=60V, the fundamental frequency of the inverter output is 50Hz, three-phase resistive-inductive load R_L=50Ω, L_L=60mH. Due to the maximum constant boost control (MCBC) method [33] has lower switching voltage stress than the simple boost control (SBC) method [1]. Therefore, in this paper, both the experimental and simulation parts will be conducted by MCBC method. In addition, all the elements used in this simulation part are assumed to be lossless.

In order to output the ac 110Vrms phase voltage from 60V dc input by using MCBC method, a shoot-through duty cycle D=0.1728 will be needed at M=0.955 for the proposed circuit. Thus, from (7), (9) and (16), we can obtain the voltage boost factor B=5.427, buck-boost factor G=MB=5.183, and the peak dc-link voltage will be V_{PN}=325.6V.

Thus, the simulation results when D=0.1728, M=0.955 and V_{dc}=60V are shown in Fig. 14. In steady-state, it can be found from Fig. 14(a) the capacitor voltages V_{C1}, V_{C2}(=V_{C3}) are pumped up to 106V and 162V, respectively. The inductor currents (i_{L1} and i_{L2}) are increased and decreased linearly during shoot-through and non-shoot-through states. The peak dc-link voltage V_{PN} is raised to 325V. Thus, the voltage boost factor B can be derived as 325/60=5.42. In Fig. 14(b), the simulated waveforms are the ac output line voltage before LC filter, output line voltage after LC filter and the harmonic spectrum of the unfiltered output line voltage V_{bc} with full range of 50kHz. Fig. 14(c) shows the output phase voltage before and after LC filter, and the ac output phase current. It can be clearly found that the ac output phase voltage leads the corresponding load current by a phase shift of 20.65°. Meanwhile, the peak value of the filtered ac output phase voltage is about 155V, then the buck-boost factor G=155/30=5.17, which is coincident with the theoretical calculated values from (16). Therefore, it can be concluded that the simulation results are fit well with the theoretical analysis.

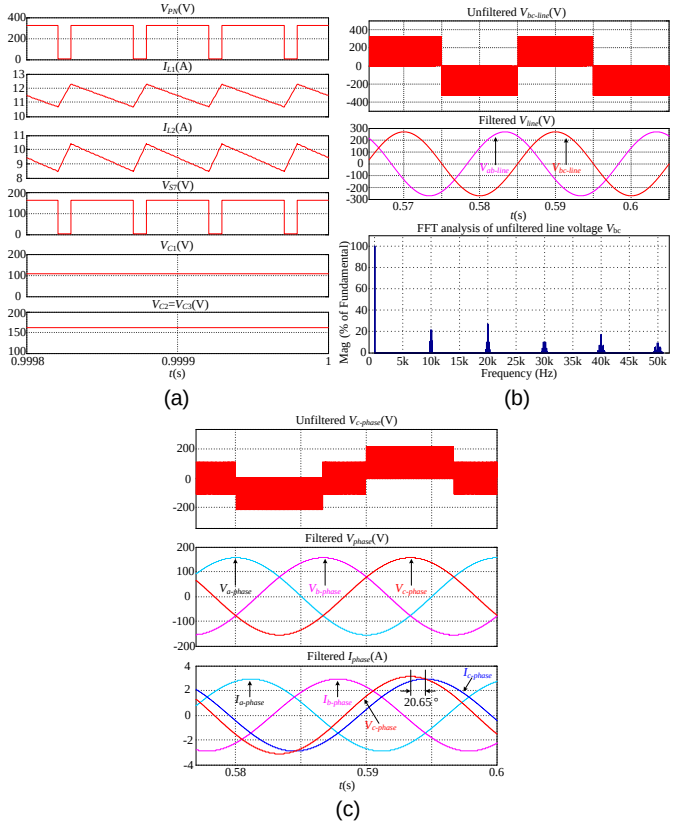


Fig. 14. Simulation results for the proposed inverter when V_{dc}=60V, D=0.1728, M=0.955. From top to bottom: (a) dc-link voltage V_{PN}, inductor currents i_{L1} and i_{L2}, drain to source voltage V_{S7}, capacitor voltages V_{C1}, V_{C2} and V_{C3}; (b) output line voltages before and after filter, FFT analysis of the unfiltered line voltage; (c) output phase voltages before and after filter, phase current.

B. Experimental Results

To verify the above simulation results and the steady-state analysis, experimental test is performed for the proposed circuit shown in Fig. 3 by using the MCBC control method. The circuit components' values and types used in the prototype are listed in Table IV. And three resistive-inductive loads (R_L=50Ω, L_L=60mH) are connected in a Y-connection at the ac output side. The PWM gate drive signals of the power switches are generated by TMS320F28335 DSP, which is 32-bit, and its clock frequency is 150MHz. All the power MOSFETs are driven by the 2BB0108T basic board with driver 2SC0108T, and the RURG3060CC are used for all the diodes.

TABLE IV
Hardware Experimental Parameters Selection

Parameters/Descriptions	Types/Values
DC input voltage	60V
Modulation index, M	0.955
Shoot-through duty cycle, D	0.1728
Switching frequency, f_s	10kHz
Fundamental frequency, f	50Hz
Inductors (L_1=L_2)	KS300125A/1mH
Capacitors (C_1=C_2=C_3)	LGU2G471MELC/470uF
LC output filter	L_f=2mH, C_f=50uF
Power MOSFET S_7	IXFH170N25X3/250V,170A
Power MOSFETs: S_1-S_6	FCH040N65S3/650V,65A
Diodes	RURG3060CC/600V, 30A
Three phase inductive loads	R_L=50Ω, L_L=60mH
DSP	TMS320F28335/32-bit,150MHz

Fig. 15 shows the measured experimental results for the proposed inverter when V_{dc}=60V, D=0.1728, M=0.955. In Fig. 15(a), from top to bottom, the waveforms are the input voltage V_{dc} and the peak dc-link voltage V_{PN}. From this figure, it can be seen that the peak dc-link voltage V_{PN} is boosted to 308V,which is a little lower than the theoretical value (5.427*60=325.6V) due to the parasitic parameters of passive and active elements (inductors, capacitors, diodes and switches). The measured experimental waveforms in Fig. 15(b) are the inductor current i_{L1}, inductor current i_{L2} and the drain-to-source voltage of switch S_7. From Fig. 15(b), it can be observed that the input current is continuous, and when all the switches are turned on, the inductor currents are increased. Otherwise, the inductor currents are decreased. The capacitor voltages are measured and shown in Fig. 15(c), it can be found that the capacitor voltages V_{C1} and V_{C2}(=V_{C3}) are pumped up to about 100V and 154V, respectively. While the theoretical calculated values from (5) are 106.5V and 162.8V, which are slightly higher than the corresponding experimental results. In Fig. 15(d), the waveforms from top to bottom are the output line voltages before LC filter and after filtering, respectively. Fig. 15(e) shows the Fast Fourier Transform (FFT) analysis of the unfiltered output line voltage V_{bc}. From this figure, it can be seen that the harmonic spectrum of the line voltage V_{bc} is mainly distributed among the switching frequency (10kHz) and its corresponding integer multiple frequencies, which fits well with the simulation results in Fig. 14 (b). In Fig. 15(f), from top to bottom, the experimental waveforms are the output phase voltage before filtering, filtered phase voltage and phase current with three-phase inductive-resistive load of R_L=50Ω and L_L=60mH, and the load current harmonic spectrum. The measured rms value of the ac output phase voltage is about 108V, as shown in Fig. 15(f), which is a little lower than the desired value, due to the parasitic effect of active/passive elements. In addition, it can be clearly found that the filtered phase voltage leads the corresponding load current by a phase shift of 20.45°. And from the load current harmonic spectrum in Fig. 15(f), the measured total harmonic distortion(THD) of this phase current is about 2.39%.

In addition, when D=0.1728, M=0.955, Fig. 16 shows the dynamic response when the input voltage V_{dc} is changed from 40V to 72V. From top to bottom, it shows the dc input voltage

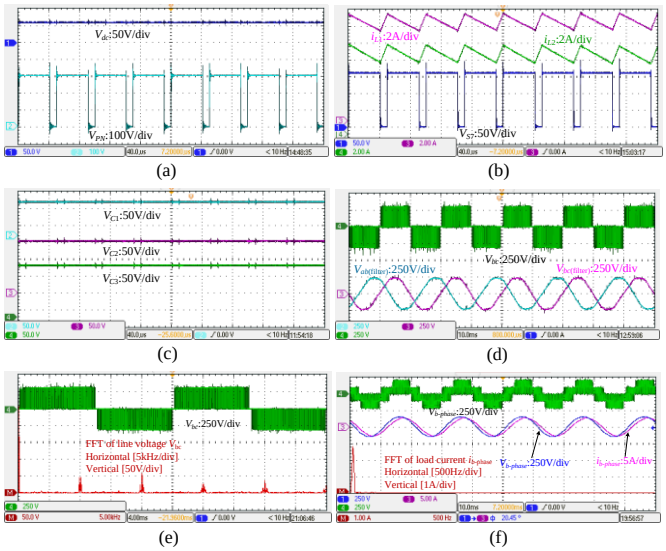


Fig. 15. Experimental results for the proposed inverter when V_{dc}=60V, D=0.1728, M=0.955. From top to bottom, (a) input voltage V_{dc}, dc-link voltage V_{PN}; (b) inductor currents i_{L1}, i_{L2}, drain-to- source voltage V_{S7}; (c) capacitor voltages V_{C1}, V_{C2}, V_{C3}; (d) output line voltage before and after filter; (e) unfiltered line voltage at 4ms, and its corresponding harmonic spectrum; (f) output phase voltage before and after filter, load current, and the load current harmonic spectrum.

V_{dc}, capacitor voltage V_{C1}, capacitor voltage V_{C2} and the peak dc-link voltage V_{PN}. From Fig. 16, it can be seen that the capacitor voltage V_{C1} would change from 60V to 120V, V_{C2} would change from 98V to 180V, and the peak dc-link voltage V_{PN} would change from 200V to 360V.

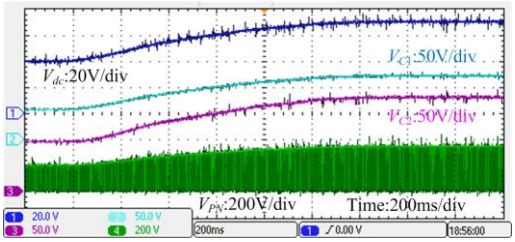
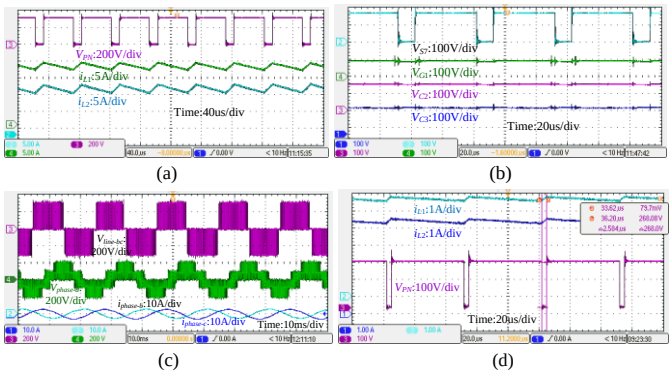
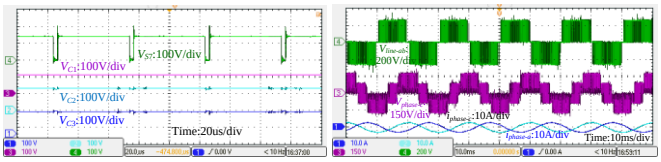


Fig. 16 Experimental dynamic response when D=0.1728, M=0.955, while the input voltage V_{dc} is changed from 40V to 72V.

Besides, in order to output the ac 110Vrms phase voltage from 40V dc input by using MCBC method, the shoot-through duty cycle D=0.2147 will be required at M=0.9068 for the proposed inverter. Fig. 17 shows the experimental results when V_{dc}=40V, D=0.2147 and M=0.9068. From Fig. 17(a), it can be seen that the peak dc-link voltage V_{PN} is raised to 320V, which is slightly less than the theoretical value 342.8V due to the voltage drop on passive and active elements. The capacitor





(e) (f)

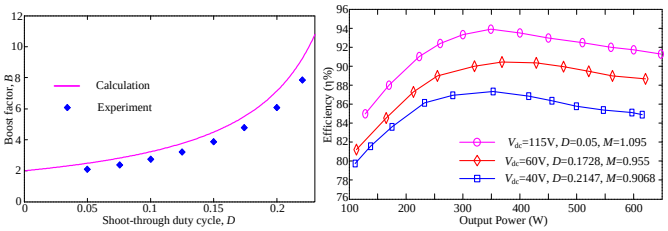
Fig. 17 Experimental results for the proposed inverter when V_{dc}=40V, D=0.2147, M=0.9068 and V_{dc}=115V, D=0.05, M=1.095. (a, d) dc-link voltage, inductor currents i_{L1}, i_{L2}; (b, e) drain-to- source voltage V_{S7}, capacitor voltages V_{C1}, V_{C2}, V_{C3}; (c, f) output line voltage $V_{line-bc}$ and phase voltage $V_{phase-a}$ before filter, and phase current $i_{phase-b}$, $i_{phase-c}$.

voltages V_{C1}, V_{C2}(=V_{C3}) are pumped up to 89V and 159V, as shown in Fig. 17(b), which are lower than the calculated values 97.8V and 171V, respectively. Additionally, the ac-side experimental waveforms, including the unfiltered line voltage $V_{\text{line-bc}}$, unfiltered phase voltage $V_{\text{phase-a}}$, and the load phase currents are measured and shown in Fig. 17(c), respectively, which shows a good agreement with the theoretical analysis.

To prove that the proposed inverter can operate at a small shoot-through duty cycle. Another set of experimental results with D=0.05 is measured. In this case, the modulation index M=1.095, and the dc input voltage will be required as V_{dc}=115V to output the ac 110Vrms phase voltage. Then, the corresponding experimental results are measured and shown in Fig. 17(d)-(f). From Fig. 17(d) and Fig. 17(e), the peak dc-link voltage V_{PN} and capacitor voltages V_{C1}, V_{C2}(=V_{C3}) are boosted to 268V, 113V and 134V, respectively, which are slightly lower than the theoretical calculated values 285V, 128V and 142.8V due to the internal parasitic parameters of active/ passive devices. The corresponding ac output phase current, phase voltage and line voltage are also measured and presented in Fig. 17(f), respectively. Besides, the shoot-through duty cycle of Fig. 17(d) can be calculated as D=2.584us/50us≈0.051, which is almost identical to the desired duty cycle value.

The calculated and the experimental boost factor values of the proposed circuit is depicted and compared in Fig. 18(a). From this figure, it can be clearly found that the experimental results are lower than that of the calculated values because the parasitic effects of the passive/active elements are ignored in theoretical calculation, while these cannot be neglected in practical occasions. In addition, the difference between the experimental results and the calculated values are increased when the shoot-through duty cycle D is increasing. This is due to the fact that the conduction losses of components will be high when the shoot-through time interval is large, which exists in all kinds of impedance source inverters.

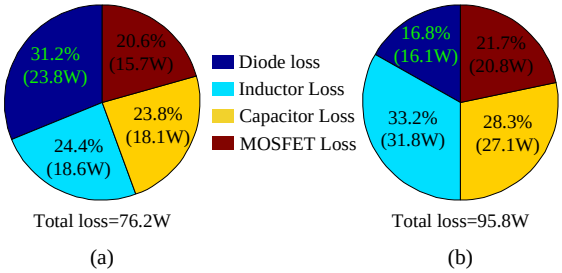
The experimental efficiency of the proposed inverter, are measured and plotted in Fig. 18(b), with different output power under V_{dc}=60V, V_{dc}=40V and V_{dc}=115V. When V_{dc}=60V, the measured maximum efficiency of the proposed inverter is about 90.3% at the load power of 367W. In order to output the ac 110Vrms phase voltage from V_{dc}=40V, a larger shoot-through duty cycle D=0.2147 will be required, then the corresponding input current of the proposed inverter at V_{dc}= 40V will be further increased and higher than that of V_{dc}=60V, which leads to the high conduction power losses on active and passive components. As a result, the measured experimental efficiency is decreased when the dc input voltage is low.



(a) (b)

Fig. 18 (a) Boost factor comparison between calculated and experimental values, (b) Measured efficiency comparison between V_{dc}=60V, V_{dc}=40V and V_{dc}=115V under different output power.

Based on the detailed power loss analysis in Section V and the loss-related parameters in Table III. The calculated loss distribution in the devices when the output phase voltage V_o=110Vrms between V_{dc}=60V and V_{dc}=40V have been shown and compared in Fig. 19. From Fig. 19(a), when V_{dc}=60V, D=0.1728, M=0.955, it can be observed that the major losses come from diodes, and its loss percentage is about 31.2%, the total power loss is about 76.2W. While, for the input voltage V_{dc}=40V, M=0.9068, the shoot-through duty cycle D is increased to 0.2147. Then, the corresponding loss distribution is calculated and shown in Fig. 19(b). It can be seen from this figure that the diode power loss is relatively small, the power losses in inductors and capacitors are more significant, and their loss percentages are 33.2% and 28.3%, respectively. The total power loss is about 95.8W, which is higher than that of the V_{dc}=60V. This is because the conduction power loss is increased when the proposed inverter operates at a large shoot-through time interval.



(a) (b)

Fig. 19 Calculated power loss distribution in the devices under the same output power P_o=570W, and switching frequency f_s=10kHz, (a) V_{dc}=60V, D= 0.1728, M=0.955, (b) V_{dc}=40V, D=0.2147, M=0.9068.

VII. CONCLUSIONS

This paper presents a new high boost non-isolated quasi-Z-source inverter with an active switched Z-impedance network, which has the following main characteristics: inrush current suppression at startup, high boost voltage inversion capability, continuous input current, and shares the same ground between the main bridge inverter and the input source. Comparison to the traditional enhanced boost (q)ZSIs (EB-ZSI and EB-qZSI), by using two less inductors, one less capacitor and one extra power switch at the impedance network, the output voltage boost factor of the proposed inverter is twice as much as the EB-ZSI and EB-qZSI. For the same dc input and ac output voltages, the proposed topology has higher modulation index to output improved waveform quality, lower passive component voltage ratings, lower shoot-through current stress flow to the inverter bridge, and has lower active switching voltage stresses.

Therefore, the low voltage rating active power switches, diodes and capacitors can be applied to this circuit, which would reduce the inverter's size and loss to some extent. As a result, the efficiency of the proposed inverter can be accordingly improved. The simulation and experimental results with 60V dc input and ac 110Vrms phase output have verified that the proposed inverter has high step-up voltage inversion capability with continuous input current. Thence, it would be suitable for the renewable power generation systems, where the low dc input voltages need to be inverted to the high level ac output.

APPENDIX

For simplicity, we assume that L_1=L_2=L and C_1=C_2=C_3=C in the impedance network. Here, we define the inductor currents i_L, capacitor voltages u_C and the load current i_{ld} as the state variables. By using the similar small-signal analysis method in [23], and after Laplace transformation, the ac small-signal transfer functions of the proposed qZSC can be derived in (A1), where I_{ld}=(1-D)V_{PN}/R_{ld}, is the average load current in steady state during a switching cycle.

Due to the dc-link voltage V_{PN}=2V_{C2}. Therefore, from (A1),

$$\begin{cases} sL_1\hat{i}_{L_1}(s)=\hat{u}_{dc}(s)+\left(V_{C_1}+V_{C_2}\right)\hat{d}(s)+D\hat{u}_{C_2}(s)-(1-D)\hat{u}_{C_1}(s) \\ sL_2\hat{i}_{L_2}(s)=2V_{C_2}\hat{d}(s)+\hat{u}_{C_1}(s)-(1-2D)\hat{u}_{C_2}(s) \\ sC_1\hat{u}_{C_1}(s)=-\hat{i}_{L_2}(s)+(1-D)\hat{i}_{L_1}(s)-I_{L_1}\hat{d}(s) \\ 2sC_2\hat{u}_{C_2}(s)=-D\hat{i}_{L_1}(s)+(1-2D)\hat{i}_{L_2}(s)-\left(I_{L_1}+2I_{L_2}-2I_{ld}\right)\hat{d} \\ \qquad\qquad -2(1-D)\hat{i}_{ld}(s) \\ \left(sL_{ld}+R_{ld}\right)\hat{i}_{ld}(s)=2(1-D)\hat{u}_{C_2}(s)-2V_{C_2}\hat{d}(s) \end{cases} \quad \text{(A1)}$$

the control $d(s)$ to the capacitor voltage $u_{C2}(s)$ transfer functions of the simplified qZSC converter can be derived as:

$$G_{vd}(s)=\left.\frac{\hat{u}_{C_2}(s)}{\hat{d}(s)}\right|_{\hat{u}_{dc}(s)=0}=\frac{b_5s^5+b_4s^4+b_3s^3+b_2s^2+b_1s}{a_6s^6+a_5s^5+a_4s^4+a_3s^3+a_2s^2+a_1s} \quad \text{(A2)}$$

where $a_6=2L_{ld}L^2C^3$, $a_5=2R_{ld}L^2C^3$, $a_3=\left(5-8D+7D^2\right)R_{ld}LC^2$,

$$\begin{cases} a_4=\left(5-8D+7D^2\right)L_{ld}LC^2+4(1-D)^2L^2C^2 \\ a_2=4(1-D)^2\left(2-2D+D^2\right)LC+\left[D^2+(1-D)^2(1-2D)^2\right]L_{ld}C \\ \qquad -\left[2D(1-D)(1-2D)\right]L_{ld}C \\ a_1=\left[D^2+(1-D)^2(1-2D)^2-2D(1-D)(1-2D)\right]R_{ld}C \end{cases}$$

$$\begin{cases} b_5=\left(2I_{ld}-I_{L1}-2I_{L2}\right)L_{ld}L^2C^2 \\ b_4=2V_{C2}(1-2D)L_{ld}LC^2+\left(2I_{ld}-I_{L1}-2I_{L2}\right)R_{ld}L^2C^2 \\ \qquad +4(1-D)V_{C2}L^2C^2-D\left(V_{C1}+V_{C2}\right)L_{ld}LC^2 \\ b_3=R_{ld}LC^2\left[2(1-2D)V_{C2}-D\left(V_{C1}+V_{C2}\right)\right]-\left(1-D-D^2\right)I_{L1}L_{ld}LC \\ \qquad +\left(2I_{ld}-I_{L1}-2I_{L2}\right)\left(2-2D+D^2\right)L_{ld}LC \\ b_2=2(1-D)L_{ld}CV_{C2}\left(1-4D+2D^2\right)+L_{ld}C\left(V_{C1}+V_{C2}\right)\left(1-4D+2D^2\right) \\ \qquad -R_{ld}LCI_{L1}\left(1-3D+D^2\right)+4(1-D)V_{C2}LC(2-2D+D^2)+ \\ \qquad\quad \left(2I_{ld}-I_{L1}-2I_{L2}\right)\left(2-2D+D^2\right)R_{ld}LC \\ b_1=R_{ld}C\left(1-4D+2D^2\right)\left[V_{C1}+(3-2D)V_{C2}\right] \end{cases}$$

REFERENCES

[1] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[2] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1453–1463, Jul. 2007.

[3] W. Song, Y. Zhang, X. Sun, Q. Zhang, and W. Wang, "A study of Z-source dual-bridge matrix converter immune to abnormal input voltage disturbance and with high voltage transfer ratio," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 828–838, May 2013.

[4] L. Z. He, S. X. Duan, F. Z. Peng, "Safe-Commutation Strategy for the Novel Family of Quasi-Z-Source AC–AC Converter," *IEEE Trans. Ind. Informat.*, vol. 9, no. 3, pp. 1538–1547, Aug. 2013.

[5] Q. Y. Sun, S. Chen, L. Chen, D. Z. Ma, "Quasi-Z-Source Network-Based Hybrid Power Supply System for Aluminum Electrolysis Industry," *IEEE Trans. Ind. Informat.*, vol. 13, no. 3, pp. 1141–1151, Jun. 2017.

[6] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE Power Electron. Spec. Conf. (PESC'08)*, Jun. 2008, pp. 2743–2749.

[7] Y. Tang, S. Xie, C. Zhang, and Z. Xu, "Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 409–415, Feb. 2009.

[8] Y. Tang, S. Xie, and C. Zhang, "An improved *Z*-source inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3865–3868, Dec. 2011.

[9] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, and L. K. Siow, "Extended-boost Z-source inverters," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2642–2652, Oct. 2010.

[10] M. Zhu, K. Yu, and F. L. Luo, "Switched-inductor Z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150-2158, Aug. 2010.

[11] M. K. Nguyen, Y. C. Lim, and G. B. Cho, "Switched-inductor quasi-Z-source inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3183-3191, Nov. 2011.

[12] M.-K. Nguyen, Y. C. Lim, and J. H. Choi, "Two switched-inductor quasi z-source inverters," *IET Power Electron.*, vol. 5, no. 7, pp. 1017–1025, Aug. 2012.

[13] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, "Generalized multicell switched-inductor and switched-capacitor Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 837–848, Feb. 2013.

[14] H. Fathi and H. Madadi, "Enhanced-Boost Z-Source Inverters with Switched Z-Impedance," *IEEE Trans. on Ind. Electron.*, vol. 63, no. 2, pp. 691–703, Feb. 2016.

[15] V. Jagan, J, Kotturu, and S. Das, "Enhanced-Boost Quasi-Z-Source Inverters with Two Switched Impedance Network," *IEEE Trans. on Ind. Electron.*, vol. 64, no. 9, pp. 6885–6897, Step. 2017.

[16] W. Qian, F. Z. Peng, and H. Cha, "Trans-z-source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3453–3463, Dec. 2011.

[17] P. C. Loh, D. Li, and F. Blaabjerg, "Γ-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4880–4884, Nov. 2013.

[18] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. Town, "Y-source impedance network," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3250–3254, Jul. 2014.

[19] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "New magnetically coupled impedance (Z-) Source networks," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7419-7434, Nov. 2016.

[20] S. Mishra, R. Adda, and A. Joshi, "Inverse Watkins-Johnson topology based inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1066–1070, Mar. 2012.

[21] R. Adda, S. Mishra, and A. Joshi, "Analysis and PWM control of switched boost inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5593–5602, Dec. 2013.

[22] S. S. Nag and S. Mishra, "Current–Fed Switched Inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4680–4690, Sep. 2014.

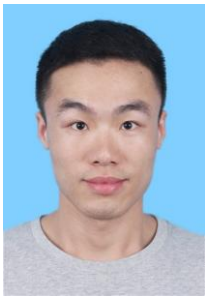
[23] M. K. Nguyen, T. V. Le, S. J. Park, and Y. C. Lim, "A class of quasi switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1526–1536, Mar. 2015.

[24] M. K. Nguyen, Y. C. Lim, and S. J. Park, "A comparison between single phase quasi-Z-source and quasi-switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6336–6344, Oct. 2015.

[25] A. -V. Ho, T.-W. Chun, and H. -G. Kim, "Extended Boost Active-Switched-Capacitor/Switched-Inductor Quasi-*Z*-Source Inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5681–5690, Oct. 2015.

[26] M. K. Nguyen, T. V. Le, S. J. Park, Y. C. Lim, and J. Y. Yoo, "Class of high boost inverters based on switched-inductor structure," *IET Power Electron.*, vol. 8, no. 5, pp. 750–759, 2015.

[27] E. Babaei, E. Shokati Asl, M. Hasan Babayi, and S. Laali, "Developed embedded switched-Z-source inverter," *IET Power Electron.*, vol. 9, no. 9, pp. 1828-1841, July 2016.
[28] M. K. Nguyen, T. D. Duong, Y. C. Lim and Y. G. Kim, "Switched Capacitor Quasi-Switched Boost Inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5105–5113, June. 2018.
[29] M.H.B. Nozadian, E. Babaei, S.H. Hosseini, and E.S. Asl, "Steady-State Analysis and Design Considerations of High Voltage Gain Switched Z-Source Inverter with Continuous Input Current," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5342–5350, July 2017.
[30] M. K. Nguyen, T. D. Duong, Y. C. Lim, J. H. Choi, "High Voltage Gain Quasi-Switched Boost Inverters with Low Input Current Ripple," *IEEE Trans. Ind. Informat.*, pp. 1-1, 2018 (early access). DOI: 10.1109/TII.2018.2806933
[31] Y. W. Gu, Y. F. Chen, B. Zhang, "Enhanced-Boost Quasi-Z-Source Inverter with An Active Switched Z-Network," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8372-8381, Oct. 2018.
[32] Y. Liu, B. Ge, H. Abu-Rub, and H. Sun, "Hybrid pulse width modulated single-phase quasi-Z-source grid-tie photovoltaic power system," *IEEE Trans. Ind. Informat.*, vol. 12, no. 2, pp. 621–632, Apr. 2016.
[33] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 770–778, May/Jun. 2006.



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