Fault Tolerant Multilevel Topology Based on Three-Phase H-Bridge Inverters for Open-End Winding Induction Motor Drives

V. Fernão Pires, *Senior Member, IEEE*, Daniel Foito, and J. Fernando Silva, *Senior Member, IEEE*

***Abstract*— In this paper, a multilevel inverter based on three-phase H-bridge inverters for an open-end winding induction motor drive is presented and its fault tolerance capability investigated. The multilevel topology is obtained using three wye-connected three-phase H-bridge inverters to supply open-end winding induction motors. This topology has the ability to extend the maximum voltage applied to the motor windings up to two times the DC supply voltage of the three-phase inverters. For a given induction motor voltage, the topology allows the use of DC sources with a lower voltage rating. Consequently faster power semiconductors can be used. This multilevel topology can be directly controlled by modifying known modulation concepts such as sinusoidal PWM. In this work two sinusoidal PWM modulation techniques will be implemented, the level shifted carriers (phase disposition) and the phase shifted modulator. Fault-tolerant operation under an open-switch fault without adding any extra components and without changing the modulation strategy is also proposed, adding fault-tolerant capability to the new topology. Experimental results of this multilevel inverter in normal operation and in fault tolerant mode are presented. The obtained results confirm the fault effectiveness of the proposed multilevel topology.**

***Index Terms*— Multilevel inverter, three-phase H-bridge converter, Sinusoidal PWM modulation, open-end winding induction motor.**

I. Introduction

LOW voltage (<1kV) AC drives use normally three-phase two-level voltage source converters (VSC), while for medium/high voltage applications multilevel VSCs have been one of the main choices. Compared to traditional two-level VSCs, multilevel VSC converters present several advantages such as, higher AC voltage levels, reduced harmonic distortion, relatively lower voltage stress on semiconductor switches, operation at reduced switching frequency, reduced voltage slew-rates and lower electromagnetic interference [1,2]. Therefore, multilevel converters became increasingly used in applications such as, flexible AC transmission systems (FACTS), HVDC transmission, high power factor rectifiers, active power filters, reactive power compensation, storage and interfaces for the renewable energy sources [2-7], and also convenient in medium and low power AC drives.

Several multilevel topologies have been proposed and implemented in industry. Three of them have been extensively studied: the neutral point clamped (NPC), the flying capacitor (FC) and the cascaded H-bridge converter topology. The NPC topology has been introduced by Nabae, Takahashi and Akagi [8]. In this topology, diodes are used as clamping devices to clamp the output voltage to the midpoint voltage of series connected capacitors dividing the input DC voltage. The FC topology [9] was introduced as an alternative for the NPC topology and uses switched capacitors to be connected or disconnected in series with the load to achieve the desired output voltage loads. These two multilevel power converters require special modulation techniques in order to achieve capacitor voltage balancing. The concept of the cascaded multilevel inverter is based on the series connection of H-bridge inverters, with separate DC sources [10]. This topology is characterized by its modular structure, simple control schemes and free from the capacitors voltage balancing problem of NPCs and FCs.

A different approach for the multilevel power converter topologies can be obtained using open-end winding induction motors. This motor is a typical induction motor with a modification to provide the 6 connections of the three stator windings (the internal neutral point connection is removed). For this kind of drives several multilevel topologies have been proposed and investigated. One of the most studied is the dual inverter configuration. This topology uses two two-level three-phase VSCs, one at each side of an open-end stator winding [11-14]. Due to the modularity of this solution, it was also used in multiphase induction motors with open-end winding [15, 16]. Since this topology if feed from two independent DC sources there is no problem with capacitor voltage balancing. Known multilevel topologies are now becoming highly used in industry. Dual inverter configuration was first presented in 1993 [11], but only in recent years a deep research has started. As a consequence, now this topology is suggested for several applications [17-19]. A multilevel inverter called hexagram inverter was also proposed for a three-phase open-end winding induction motor [20, 21]. This topology is derived from a combination of six three-phase six-switch modules. Other multilevel topologies for the open-end winding induction motor have also been proposed [22-25]. However, in these topologies the complexity of the power circuit has been significantly increased.

Under this context, this paper presents a new multilevel topology for an open-end winding induction motor. The proposed topology is modular since it combines three identical

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three-phase H-bridge inverters in wye connection (3yVSC). In this topology the maximum voltage that can be applied to the terminals of the stator can be extended to the double of the DC voltage source. It is also characterized by voltages with five levels at the terminals of the motor windings. The proposed multilevel inverter also allows the direct application of known modulation concepts such as sinusoidal PWM. In this work two SPWM modulation techniques, the level shifted carrier (phase disposition) and the phase shifted carrier, are modified to be adapted to the 3VSCY topology. Another advantage of this topology is that it allows fault tolerant operation even with known PWM modulation concepts, as shown in this paper.

II. Proposed Multilevel Open-End Winding Induction Motor Drive

Some multilevel topologies have been proposed for open-end winding induction motor drives. One of the most known and used topologies is the dual inverter configuration that involves series connection of two three-phase inverters (see Fig. 1). This concept presents the advantage of using a modular topology based on well known three-phase VSIs. The maximum voltage that can be applied to the windings is $1.33V_{DC}$ [26]. One of the drawbacks is that direct application of existing PWM modulators such as SPWM is not feasible [19], [23], [26].

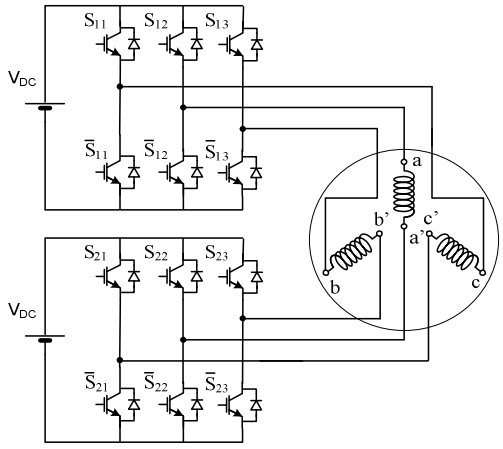

Fig. 1. Multilevel inverter based on the dual inverter configuration.

In order to extend the maximum voltage that can be applied to the windings and use known PWM modulators the new 3yVSC modular multilevel inverter topology is proposed for open-end winding induction motor drives. This topology (Fig. 2) is based in three two-level three-phase voltage source converters with separate DC sources connected in wye configuration. In each of the three-phase modules there are two AC outputs that are connected at two of the stator windings. The other output connects to the other VSIs through a neutral connection. Comparing with the previous topology (Fig. 1) the 3yVSC power converter requires an extra VSC with power source, but provides higher output maximum voltage ($2V_{DC}$ instead of 1.33 V_{DC}). Thus, the output power can be made higher or lower voltage rating DC sources can be used, allowing in this way the reduction of the switches blocking voltages for the same output power. In some situations this will allow to use MOSFETs instead of IGBTs which can be considered an important feature. Another advantage of the 3yVSC topology is the direct application of known modulation concepts such as sinusoidal PWM, even for fault tolerant operation.

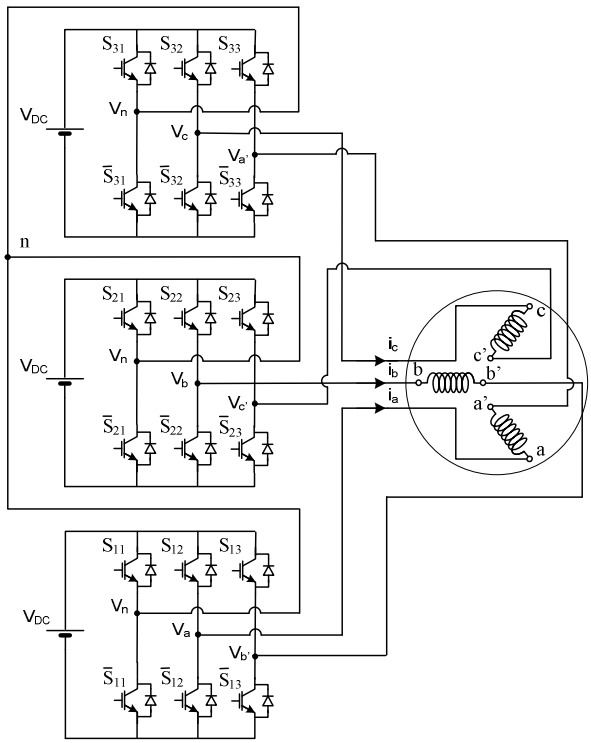

Fig. 2. Proposed multilevel topology based on three-phase H-bridge inverters.

The applied winding voltages are dependent of the states of the power switches. Considering ideal switches, their conduction state can be described by the following binary variables α_{ij} (where i and $j \in \{1,2,3\}$):

$$\alpha_{ij} = \begin{cases} 1 \text{ if } S_{ij} \text{ is ON } \wedge \ \bar{S}_{ij} \text{ is OFF} \\ 0 \text{ if } S_{ij} \text{ is OFF } \wedge \ \bar{S}_{ij} \text{ is ON} \end{cases} \quad (1)$$

From the analysis of the circuit presented in Fig. 2 and taking into consideration (1), the winding voltages can assume several voltage levels in accordance with:

$$v_{aa'} = (\alpha_{12} - \alpha_{11})V_{DC} + (\alpha_{31} - \alpha_{33})V_{DC} \quad (2)$$

$$v_{bb'} = (\alpha_{22} - \alpha_{21})V_{DC} + (\alpha_{11} - \alpha_{13})V_{DC} \quad (3)$$

$$v_{cc'} = (\alpha_{32} - \alpha_{31})V_{DC} + (\alpha_{21} - \alpha_{23})V_{DC} \quad (4)$$

From these last equations it can be verified that from the point of view of the stator windings the power converter can apply several voltage levels. In fact, five voltage levels can be obtained: $-2V_{DC}$, $-V_{DC}$, 0, $+V_{DC}$ and $+2V_{DC}$. This can be

verified for example with stator winding phase *a*. Fig. 3 shows the obtained circuit in this situation. Table 1 is based on the analysis of Fig. 3 and shows the different output voltage levels at the terminals of the motor phase a according to the possible binary combinations of the switching states. Only the combination of the first and the second legs of the first and third bridges are presented since only these legs affect the applied voltage to the motor phase *a*. Thus, from Fig. 3 and Table 1 is possible to verify that the maximum voltage at the terminals of phase *a* is obtained through a series connection of the two DC sources, allowing in this way to double the peak voltage from V_{DC} to $2V_{DC}$.

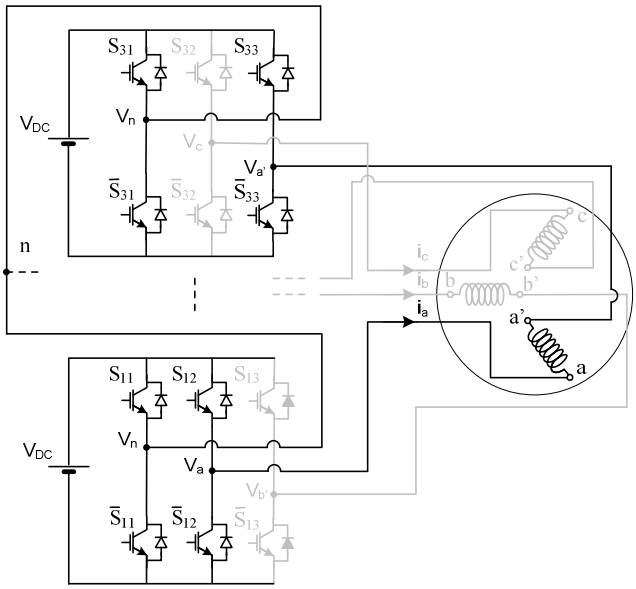

Fig. 3. Obtained circuit considering only phase *a*.

TABLE I
MOTOR PHASE A VOLTAGE ACCORDING THE SWITCHING STATES

Phase *a* voltage	Inverter 1		Inverter 3	
	S_{11}	S_{12}	S_{31}	S_{33}
$2V_{DC}$	0	1	1	0
V_{DC}	0	1	0	0
	0	1	1	1
	0	0	1	0
	1	1	1	0
0	0	0	0	0
	0	0	1	1
	1	1	0	0
	1	1	1	1
	0	1	0	1
	1	0	1	0
$-V_{DC}$	1	0	0	0
	1	0	1	1
	0	0	0	1
	1	1	0	1
$-2V_{DC}$	1	0	0	1

From the analysis of Table 1 it can be seen that there are redundant combinations associated to the voltage levels $-V_{DC}$, 0, $+V_{DC}$. This will allow to implement a fault tolerant strategy, although at reduced power since there are not redundant states associated to the voltage levels $-2V_{DC}$ and $+2V_{DC}$. One of the characteristics of the 3yVSC topology is that it allows a known sinusoidal PWM modulation technique even in fault tolerant condition.

III. MODULATION STRATEGIES

The proposed topology can be controlled by sinusoidal PWM modulation techniques, usually used in multilevel power converters. Therefore, two sinusoidal PWM modulation techniques will be implemented, the level shifted carriers (phase disposition) and the phase shifted carriers.

a) Phase disposition PWM

The operating principle of the phase disposition (PD-PWM) applied to the three-phase inverter that connects to the *a* terminal of the proposed multilevel inverter is illustrated in Fig. 4. For the remaining two inverters the sinusoidal carrier waveforms will be shifted by 120°. It is possible to verify that the operating principle is similar to PD-PWM used in multilevel inverters. A reference signal is compared to two carriers (V_{CR1} and V_{CR2}) using a simple comparison logic as can be seen in Fig. 5. From the circuit it is seen that the devices of the second and third leg are switched simultaneously in the PWM cycle. Thus, the first carrier (V_{CR1}) is used to drive the power semiconductors of the legs that are connected to the stator windings. The second carrier (V_{CR2}) is used to drive the power semiconductors of the 'neutral' leg. As expected, in each inverter three voltage levels are obtained in AC line-to-line voltages. Transposing this to the 3yVSC topology, five voltage levels are obtained since the voltage at each winding is the combination of the AC voltages of two inverters (equations 2 to 4).

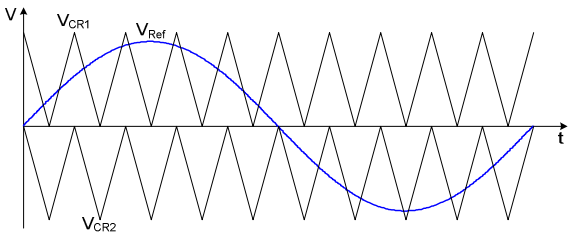

Fig. 4. Level Shifted carrier (PD-PWM) used in the proposed multilevel inverter.

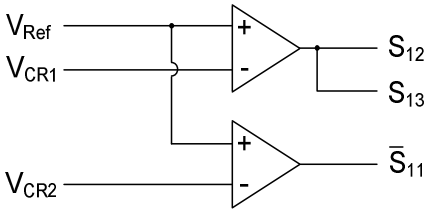

Fig. 5. Firing pulse circuit for the three-phase inverter connected to the terminal *a* (PD-PWM).

The modulation strategy associated to stator winding phase *a* is presented in Fig. 6, where reference signals V_{Ref1} is

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associated to the first and second legs of the inverter 1 and V_{Ref2} is related with first and third legs of the inverter 3 (see Fig. 3). It can be observed that the gate signals associated to the power semiconductors of phase *a* are functions of two sinusoids shifted by 120º. This is equivalent to a sinusoid which is the difference between the two references. Due to this the maximum value of the fundamental component of the windings voltage is slightly less than $2V_{DC}$, being instead given by $\sqrt{3}\,V_{DC}$.

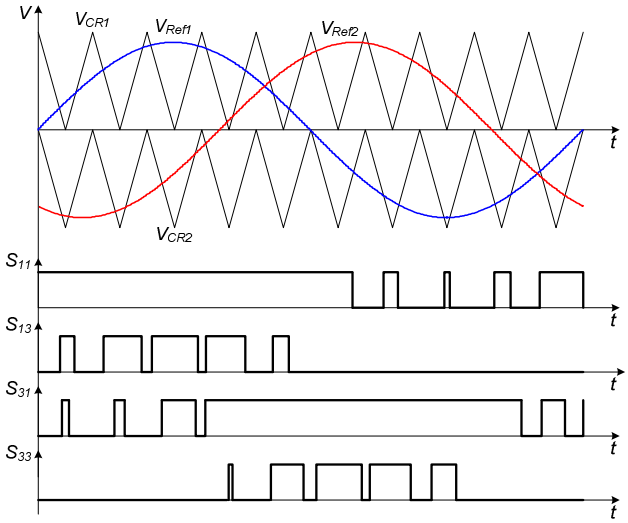

Fig. 6. PD-PWM modulation strategy associated to stator winding phase *a*.

b) Phase shifted modulator PWM

The phase shifted sinusoidal PWM modulation technique (PSM-PWM) will also be applied to the proposed 3yVSC. Fig. 7 shows the adopted scheme for this strategy used for the three-phase inverter that connects to the *a* terminal. In the practical realization only one carrier is used, but this requires the use of two reference signals that are 180º out of phase. This PWM strategy maintains the same principle of PD-PWM relatively to the devices of the second and third leg, which means they are switched simultaneously. As presented in Fig. 7, in this strategy each of the reference signals are related with different legs of each inverter. The reference signal V_{Ref1} is used to switch the power semiconductors of the legs that are connected to the stator windings. The reference signal $-V_{Ref1}$ is used to switch the power semiconductors of the 'neutral' leg. Fig. 8 shows the new firing circuit associated to the three-phase inverter connected to the terminal *a*.

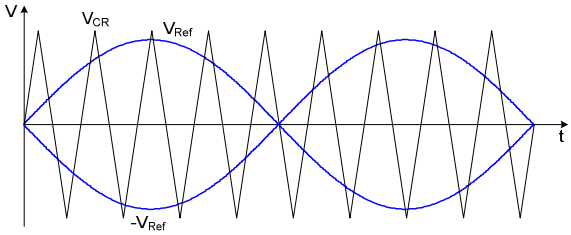

Fig. 7. Phase Shifted modulator (PSM-PWM) used in the proposed multilevel inverter.

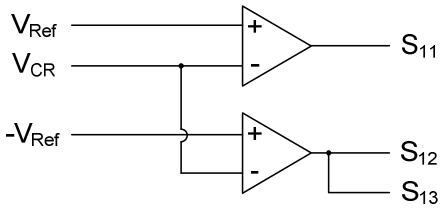

Fig. 8. Firing pulse circuit for the three-phase inverter connected to the terminal *a* (PS-PWM).

Associated to each three-phase inverter there is a change of the modulation strategy when compared with the previous one (PD-PWM). However, from the point of view of the combination of the inverters the strategy is similar since between two inverters the references are also shifted by 120º. Fig. 9 shows the modulation strategy associated to stator winding phase a, where V_{Ref1} and $-V_{Ref1}$ are associated to the inverter 1 and V_{Ref2} and $-V_{Ref2}$, shifted by 120º from V_{Ref1}, $-V_{Ref1}$, are associated with inverter 3. Thus, the maximum value of the fundamental component of the voltage across each winding it is also slightly less than $2V_{DC}$ as in the previous modulation. In fact, as described the voltage applied to the terminals of each of the windings is a result of a series connection of two inverters. Therefore, the maximum value of the voltage fundamental component is limited to $\sqrt{3}\,V_{DC}$.

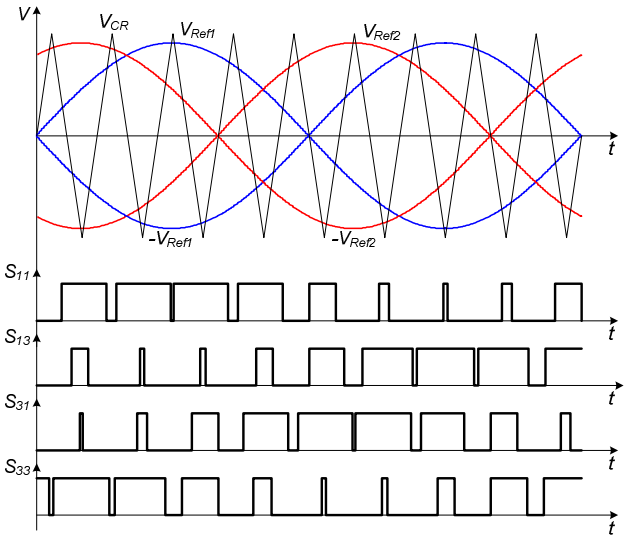

Fig. 9. PS-PWM modulation strategy associated to stator winding phase *a*.

c) Fault tolerant PWM

The proposed 3yVSC topology is also characterized by the capability of fault tolerant operation under an open switch fault without requiring any extra hardware, by simply post-processing the generated PWM pattern. In the case of an open fault, the power converter can continue operation without changing the modulation strategy being in use during the pre-fault situation. Nevertheless, the healthy switch of the leg where the open switch fault occurs must be permanently turned-on. For faults in the switches of the legs that connect to the motor, the number of controlled voltage levels that can be applied to the winding linked to the faulty leg is reduced from

five to four. The same happens with the maximum controlled voltage that can be applied to that winding, since it is reduced from $-2V_{DC}$ to $-V_{DC}$ or from $2V_{DC}$ to V_{DC}.

Since these limitations only affect the winding associated to the inverter where the fault occurs, the motor voltages will be unbalanced. To overcome this problem, the switches of the healthy inverters with the same position of the faulty switch must be permanently turned-off. Oppositely, the healthy switch of the same leg must be permanently turned-on. As an example an open switch fault for S_{12} will be considered (Fig. 2). In this fault condition the power switch $\overline{S}_{12}$ must be permanently turned-on. Also the power switches S_{22} and S_{32} of the other healthy inverters must be permanently turned-off. On other hand, the power switches of the same legs $\overline{S}_{22}$ and $\overline{S}_{32}$ must be permanently turned-on. The same should happen with the power switches of the other legs that connect to the load (S_{13} , $\overline{S}_{13}$, S_{23} , $\overline{S}_{23}$, S_{33} , $\overline{S}_{33}$). For faults in the switches of the legs that connect to the neutral wire there is the same behaviour regarding the controlled voltage levels and applied maximum voltages to the windings. However, this situation will affect two windings, more specifically those who are linked to the inverter where the fault occurs. For example for a fault in S_{11} , the windings *aa'* and *bb'* will be affected. In this situation there will be an unbalance of the motor voltages. To avoid this unbalance, the same strategy that was used for the faults in the switches of the legs that connects to the motor can be adopted. The disadvantage of this strategy is that the maximum power that can be applied to the motor is reduced. However, changes in the modulation strategy are not required between the pre and post fault and all the voltages applied to the windings will be symmetrical.

IV. Experimental Results

The proposed multilevel inverter 3yVSC topology based on the three three-phase voltage source inverters was implemented experimentally, using three isolated 100 V DC sources. The frequency of the carriers was set to 3 kHz and the frequency of the references was 60 Hz. The 3yVSC multilevel power converter feeds an induction motor with open windings.

The laboratory waveforms of the voltages and current obtained from the 3yVSC multilevel converter using the PD-PWM modulation strategy are presented in Figs. 10 and 11. Fig. 10 presents the waveforms of phase *a* to neutral voltage (V_{an}), voltage of phase *c* to neutral (V_{cn}) and phase *a* load voltage ($V_{aa'}$). The waveforms of the output voltage of the inverters 1 and 3 have only three possible output voltages ($-V_{DC}$, 0 and $+V_{DC}$). However, the load voltage has five possible output voltages ($-2V_{DC}$, $-V_{DC}$, 0, $+V_{DC}$ and $+2V_{DC}$) since this waveform is the difference between the voltages of inverter 1 and inverter 3. This shows the multilevel operation of the system, and that the magnitude of load voltage is the double of the DC voltage source. Fig. 11 shows the waveforms of the load currents. The distortion of these currents is very low due to the multilevel voltages applied to the load.

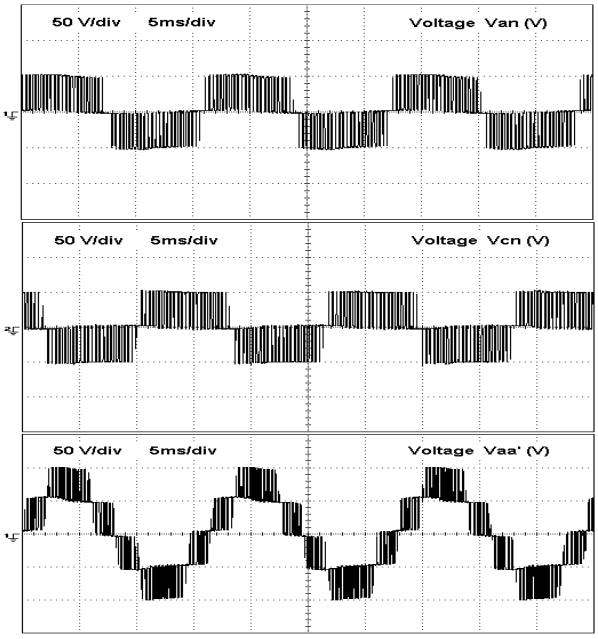

Fig. 10. Experimental voltage waveforms using PD-PWM.

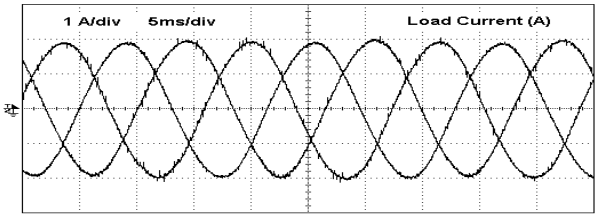

Fig. 11. Current waveforms using PD-PWM.

Fig. 12 shows a spectrum analysis of the load voltage ($V_{aa'}$) for this modulation strategy (PD-PWM). It shows that the significant harmonics are located around the carrier frequency and multiples of this. The measured total harmonic distortion (THD) of the unfiltered load voltage (THDv) was THDv = 36%. The THD value for the load current was THDi = 3.95%, confirming the low distortion of the load current, obtained without any extra filtering.

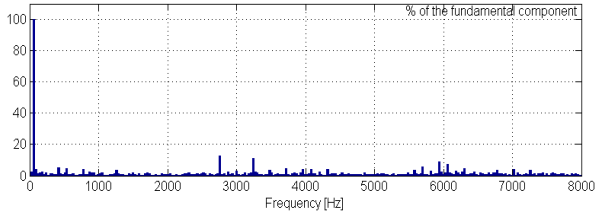

Fig. 12. Load voltage spectrum using PD-PWM.

Using the PSM-PWM modulation strategy distinct waveforms of the load voltages can be obtained. In fact, this can be confirmed in Fig. 13 where the waveforms of the voltages obtained with the use of the PSM-PWM modulation strategy are presented. The number of levels and amplitude of the voltage of phase *a* to neutral voltage (V_{an}), voltage of phase *c* to neutral (V_{cn}) and phase *a* load voltage ($V_{aa'}$) are the same 3 levels. However, it is clear from this figure that the

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shape of the load voltage is significantly different than the one that was obtained with the PD-PWM modulation. The load current waveforms are presented in Fig. 14. As can be seen by this figure the load currents still maintain a low distortion.

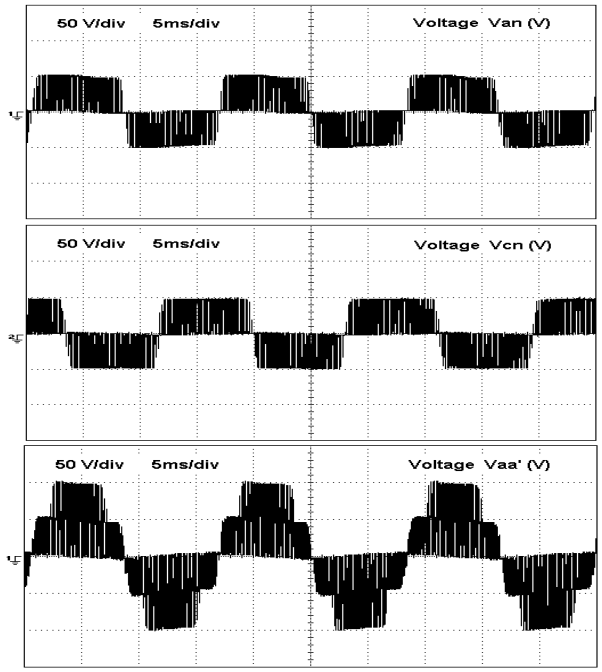

Fig. 13. Experimental voltage waveforms using PSM-PWM.

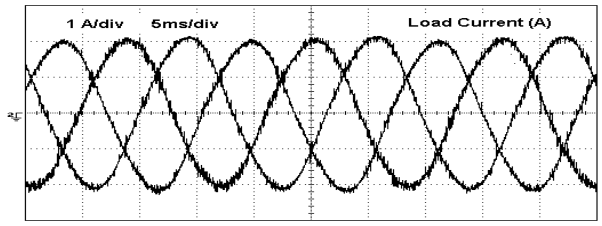

Fig. 14. Current waveforms using PSM-PWM.

The resultant harmonic spectrum of the Fig. 13 load voltage is shown in Fig. 15. This experimental result confirms that with this modulation technique the significant harmonics are concentrated around the double of the carrier frequency. In this test it was obtained 72 % for the THDv of the load voltage. For the load current was obtained a THDi of 5.64 %.

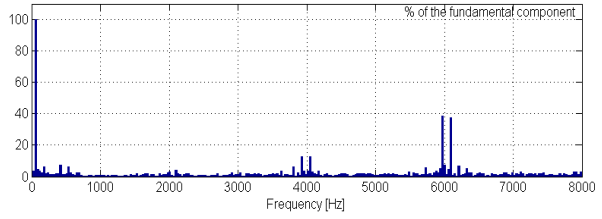

Fig. 15. Load voltage spectrum using PSM-PWM.

Comparing the results of both modulation strategies it is possible to verify that for the same frequency modulation index and considering the load voltage waveform, the equivalent switching frequency in the PSM-PWM is higher than in the PD-PWM. In fact, with this modulation strategy the load voltage effective switching frequency is the double of the switching frequency of each leg of the inverters. However, taking into consideration the load voltage THD, the PD-PWM allowed to obtain a lower THDv value since the amplitude of the double switching frequency harmonics of PSM-PWM is more than two times greater than in PD-PWM.

The behavior of the 3yVSC topology with the two tested modulation strategies under open transistor fault was also tested. Fig. 16 shows the transient waveforms of the voltage of phase a to neutral (V_{an}), voltage of phase c to neutral (V_{cn}) and phase *a* load voltage ($V_{aa'}$) in normal operation and with S_{12} open transistor fault (after t = 25ms) using PD-PWM. The figure shows that voltages related with phase *a* are affected, namely they become unbalanced and with a limitation of the number of voltage levels. Fig. 17 shows the load currents for the same condition. This figure shows that after the fault the currents also become unbalanced, with a high distortion of phase *a* current and with a DC component. These problems are related with the fact that the modulation scheme was not changed to the fault tolerant PWM after the fault.

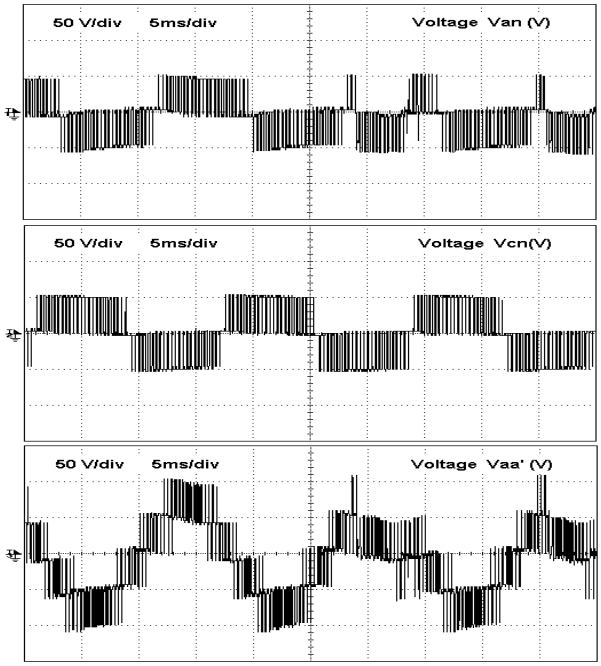

Fig. 16. Experimental voltage waveforms using PD-PWM before and after S_{12} open fault.

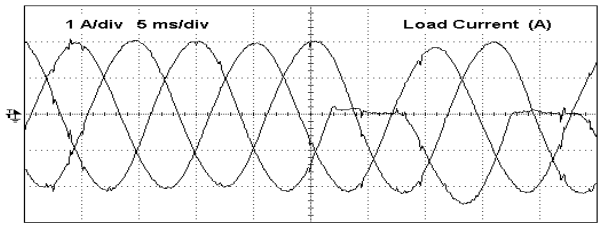

Fig. 17. Experimental current waveforms using PD-PWM before and after S_{12} open fault.

Fig. 18 shows the waveforms of the voltage of phase *a* to neutral (V_{an}), voltage of phase *c* to neutral (V_{cn}) and phase *a*

load voltage ($V_{aa'}$) under S_{12} open switch fault using the PD-PWM and the fault tolerant PWM strategy referred in the previous section (III c)). The number of levels is reduced from three to two and from five to three relatively to phase to neutral voltage and load voltage respectively. The phase to neutral voltages lose their symmetry and present a DC component. The voltage phase *a* to neutral (V_{an}) and phase *c* to neutral remain 120° out of phase. The output voltage presents symmetry and no DC component. The load currents in this fault condition are presented in Fig. 19 to show that in this condition these currents present some distortion. In this test after the fault it was used the fault tolerant PWM strategy. Therefore, the problems associated to an open transistor fault (as verified in the previous test) were minimized.

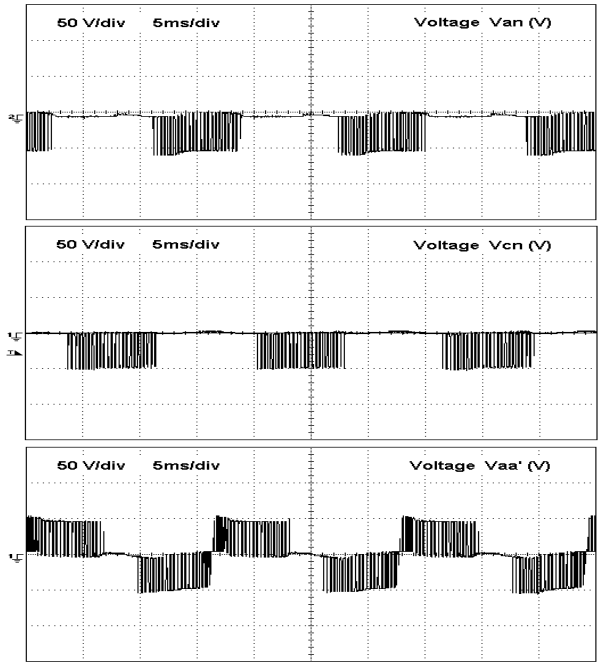

Fig. 18. Experimental voltage waveforms using PD-PWM under S_{12} open fault.

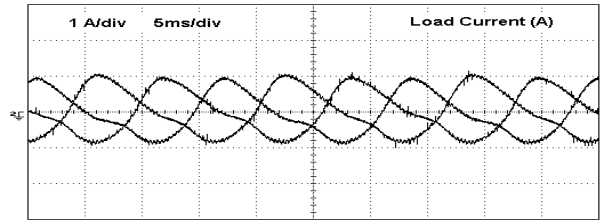

Fig. 19. Experimental current waveforms using PD-PWM under S_{12} open fault.

The same test was made, but in this case it was used the PSM-PWM modulation strategy. Fig. 20 shows the obtained waveforms of the voltage of phase *a* to neutral (V_{an}), the voltage of phase *c* to neutral (V_{cn}) and phase *a* load voltage ($V_{aa'}$). As can be seen in this figure, as it happened with the previous test, the number of levels is also reduced from three to two and from five to three relatively to phase to neutral voltage and load voltage respectively. However, the waveforms of the phase to neutral voltages are different from the previous test although still presenting a DC component. On other hand, the output voltage presents a better quality when compared to the previous test. From the analysis of the obtained load currents (Fig. 21) it can be concluded that in this case the distortion is very low.

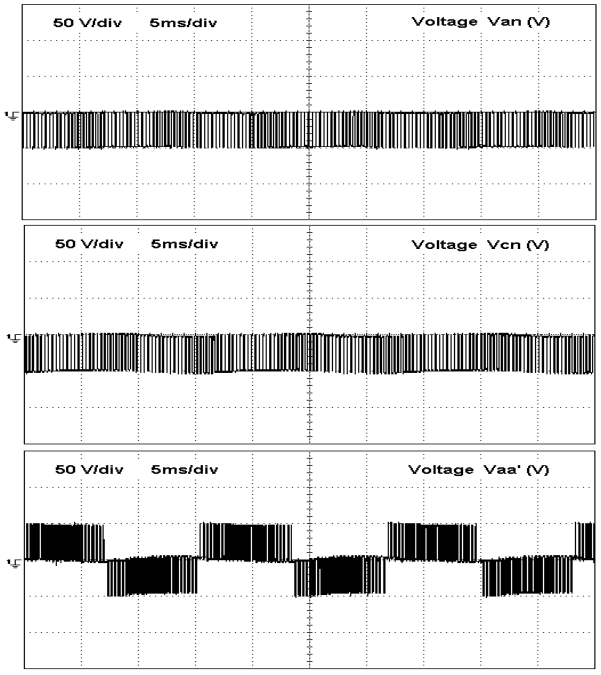

Fig. 20. Waveforms using PSM-PWM under S_{11} open fault a) Load voltage of phase $a - V_{aa'}$ b) Load current of phase $a - i_a$.

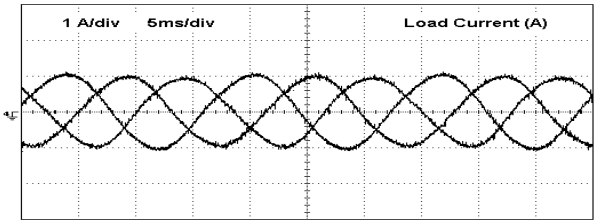

Fig. 21. Current waveforms using PSM-PWM.

Comparing the obtained results for both modulation strategies under open switch fault, it can be said that the PSM-PWM modulator presents better characteristics regarding the output voltages and currents.

V. CONCLUSIONS

A new type of multilevel inverter for an open-end winding induction motor drive was presented. The 3yVSC topology is designed in order to use existing three-phase H-bridge inverters. More specifically, the topology uses three power converters connected in wye configuration. This multilevel arrangement is capable of producing a load voltage with five possible output voltages and with the double of the DC voltage sources. The 3yVSC topology is also characterized by the possibility of using known modulation concepts such as sinusoidal PWM. In this work the PD-PWM and the PSM-PWM were implemented. The characteristics and performance of the proposed 3yVSC topology were confirmed through experimental results. The use of two modulation

strategies results in different characteristics of the load voltages. For the same frequency modulation index the equivalent switching frequency that is obtained for the load voltage with the PSM-PWM is double than the one obtained with the PD-PWM. However, when using the PD-PWM lower values for the THD load voltage were obtained. The 3yVSC topology was also analysed under open switch fault conditions without changing the modulation technique, but just inhibiting the PWM signals of certain power semiconductors. From this analysis it was verified that the continuous operation is feasible although at reduced output power. The fault condition was also analysed for both modulation strategies. Using the 3yVSC with PSM-PWM modulation enabled better results for the load current THD when compared to higher values obtained from PD-PWM.

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REFERENCES

[1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, M. A. M. Prats, "The age of multilevel converters arrives", IEEE Industrial Electronics Magazine, Issue 2, pp. 28-39, June 2008.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters", IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553-2580, August 2010.

[3] F. Khoucha, M. S. Lagoun, A. Kheloui, M. Benbouzid, "A Comparison of Symmetrical and Asymmetrical Three-Phase H-Bridge Multilevel Inverter for DTC Induction Motor Drives", IEEE Transactions on Energy Conversion, vol. 26, no. 1, pp. 64-72, March 2011.

[4] N. M. R. Santos, J. F. Silva, J. Verveckken, V. F. Pires, R. Castro, "Enhancing the Ride-Through Capability of DC-Link Voltage in NPC Multilevel Unified Power-Flow Controllers", IEEE Transactions on Power Delivery, vol. 29, no. 4, pp. 1542-1550, August 2014

[5] Q. Hao, B.-T. Ooi, F. Gao, C. Wang, N. Li, "Three-Phase Series-Connected Modular Multilevel Converter for HVDC Application", IEEE Transactions on Power Delivery, vol. 31, no. 1, pp. 50-58, February 2016.

[6] P. Samuel, R. Gupta, D. Chandra, "Grid Interface of Wind Power With Large Split-Winding Alternator Using Cascaded Multilevel Inverter", IEEE Transactions on Energy Conversion, vol. 26, no. 1, pp. 299-309, March 2011.

[7] L. V. Nguyen, H.-D. Tran, T. T. Johnson, "Virtual Prototyping for Distributed Control of a Fault-Tolerant Modular Multilevel Inverter for Photovoltaics", IEEE Transactions on Energy Conversion, vol. 29, no. 4, pp. 841-850, December 2014.

[8] A. Nabae, I. Takahashi, H. Akagi, "A new neutral-point clamped PWM inverter", IEEE Transactions on Industrial Applications, vol. IA-17, no. 5, pp. 518–523, September 1981.

[9] T. A. Meynard, H. Foch, "Multi-level choppers for high voltage applications", European and Power Electronics and Drives Journal, vol. 2, no. 1, pp. 45–50, March 1992.

[10] R. H. Baker and L. H. Bannister, "Electric power converter," U.S. Patent 3 867 643, Feb. 1975.

[11] H. Stemmler, P. Guggenbach, "Configurations of high-power voltage source inverter drives", European Conference on Power Electronics and Applications, vol. 5, pp. 7-14, September 1993.

[12] K.A Corzine, S.D. Sudhoff, C.A. Whitcomb, "Performance characteristics of a cascaded two-level converter", IEEE Transactions on Energy Conversion, vol. 14, n. 3, pp. 433-439, September 1999.

[13] M. R. Baiju, K. K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," IEEE Trans. Power Electron. vol. 19, no. 3, pp.794-805, May 2004.

[14] X. Kou, K. A. Corzine, M. W. Wielebski, "Overdistention Operation of Cascaded Multilevel Inverters," IEEE Trans. Industrial Applications, vol. 42, no. 3, pp.817-824, May/June 2006.

[15] E. Levi, I N. W. Satiawan, N. Bodo, M. Jones, "A Space-Vector Modulation Scheme for Multilevel Open-End Winding Five-Phase Drives", IEEE Transactions on Energy Conversion, vol. 27, no. 1, pp. 1-10, March 2012.

[16] M. Darijevic, M. Jones, E. Levi, "An Open-End Winding Four-Level Five-Phase Drive", IEEE Transactions on Industrial Electronics, vol. 63, no. 1, pp. 538-549, January 2016.

[17] B. A. Welchko and J. M. Nagashima, "A comparative evaluation of motor drive topologies for low-voltage, high-power EV/HEV propulsion systems," IEEE International Symposium on Industrial Electronics, pp. 379–384, June 2003.

[18] G. Grandi, C. Rossi, A. Lega, and D. Casadei, "Multilevel operation of a dual two-level inverter with power balancing capability," 41st IAS Annual Meeting. Conference Industry Applications Conference, pp. 603–610, October 2006.

[19] M. Darijevic, M. Jones, E. Levi, "An Open-End Winding Four-Level Five-Phase Drive", IEEE Transactions on Industrial Electronics, vol. 63, no. 1, pp. 538-549, January 2016.

[20] J. Wen, K. Smedley, "A New Multilevel Inverter – Hexagram Inverter for Medium Voltage Adjustable Speed Drive Systems Part II. Three-phase Motor Drive", IEEE Power Electronics Specialists Conference, pp. 1571-1577, June 2007.

[21] L. Zhou, K. Smedley, "Postfault Control Strategy for the Hexagram Inverter Motor Drive", IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2719-2729, August 2010.

[22] V. T. Somasekhar, K. Gopakumar, M. R. Baiju, K. K. Mohapatra, L. Umanand, "A Multilevel Inverter System for an Induction Motor With Open-End Windings," IEEE Trans. on Industrial Electronics, vol. 52, no. 3, pp.824-836, June 2005.

[23] K. A. Corzine, M. W. Wielebski, F. Z. Peng, J. Wang, "Control of Cascaded Multilevel Inverters," IEEE Trans. Power Electron., vol. 42, no. 3, pp.732-738, May 2004.

[24] P. P.Rajeevan, K. Sivakumar, K. Gopakumar, C. Patel, H. Abu-Rub, "A Nine-Level Inverter Topology for Medium Voltage Induction Motor Drive with Open-end Stator Winding," IEEE Trans. on Industrial Electronics, vol. 60, no. 9, pp.3627-3636, September 2013.

[25] B. V. Reddy, V. T. Somasekhar, "A Dual Inverter Fed Four-Level Open-End Winding Induction Motor Drive With a Nested Rectifier-Inverter," IEEE Trans. on Industrial Informatics, vol. 9, no. 2, pp.938-946, May 2013.

[26] G. Grandi, D. Ostojic, "Carrier-Based Discontinuous Modulation for Dual Three-Phase Two-Level Inverters", International Symposium on Power Electronics, Electrical Drives, Automation and Motion, pp. 839-844, June 2010.